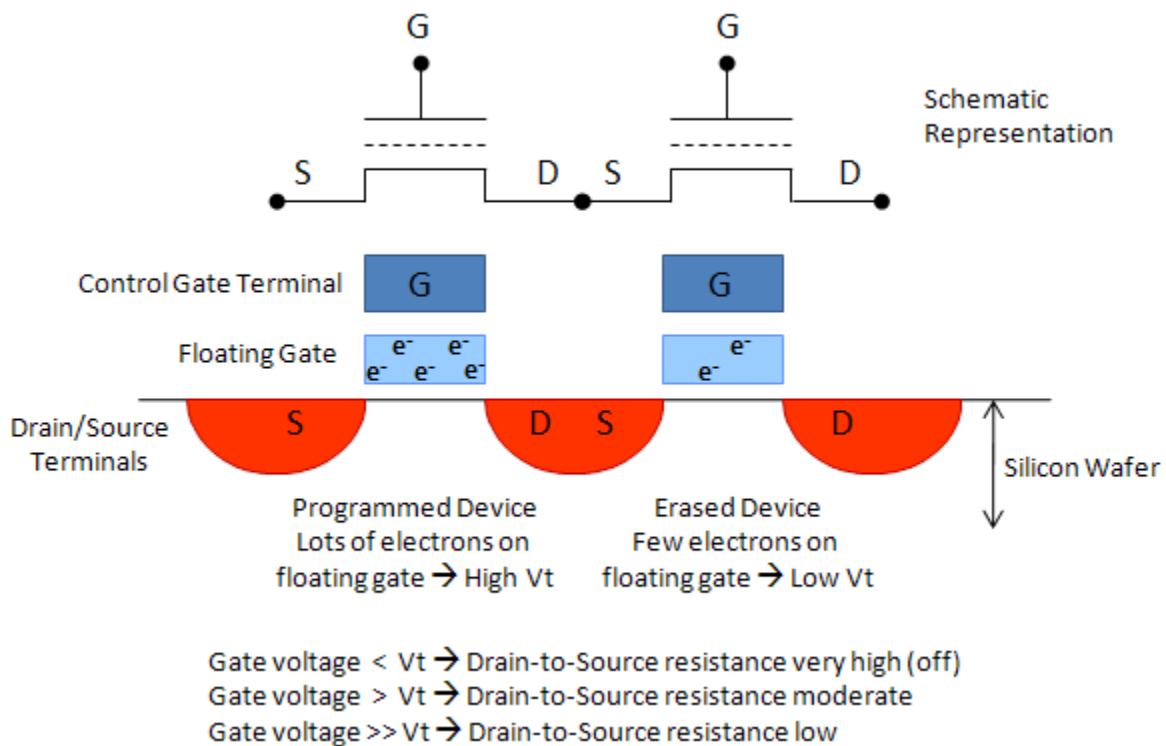
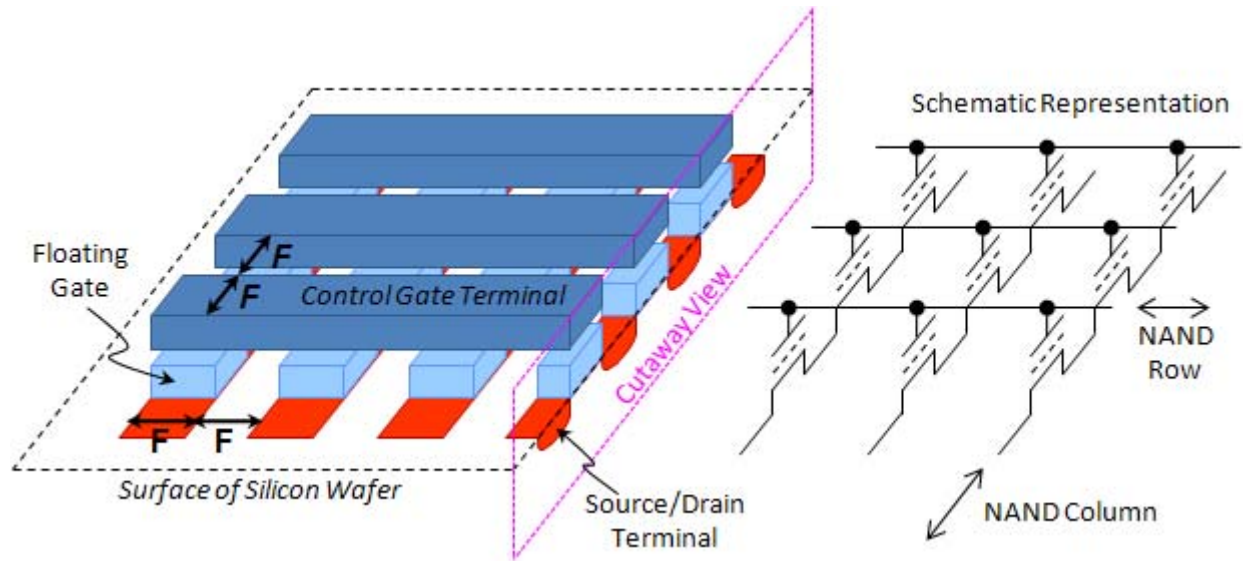


Why CMOx™ Cross-Point Memory Arrays?

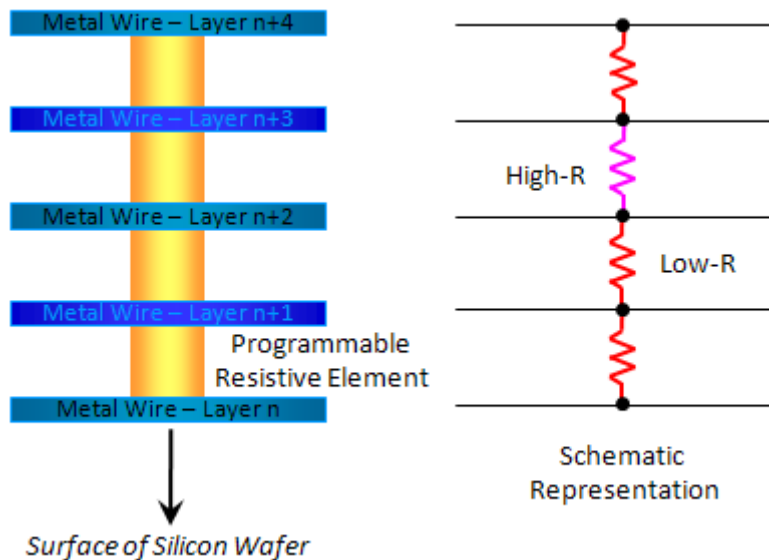
Conventional NAND-Flash memory technology uses a Floating-Gate MOS Field-Effect Transistor as the storage element for data. The MOSFET is a 3-terminal device where the voltage applied to the Gate terminal modulates the resistance seen between the Drain and the Source terminals. In the Floating-Gate implementation, the On-Off switching voltage (V_t) of the Gate terminal can be adjusted up or down in voltage by adding (program) or removing (erase) electrons to or from the floating gate. This allows data to be stored in the device as determined by the value of the On-Off switching voltage that is programmed into the device.



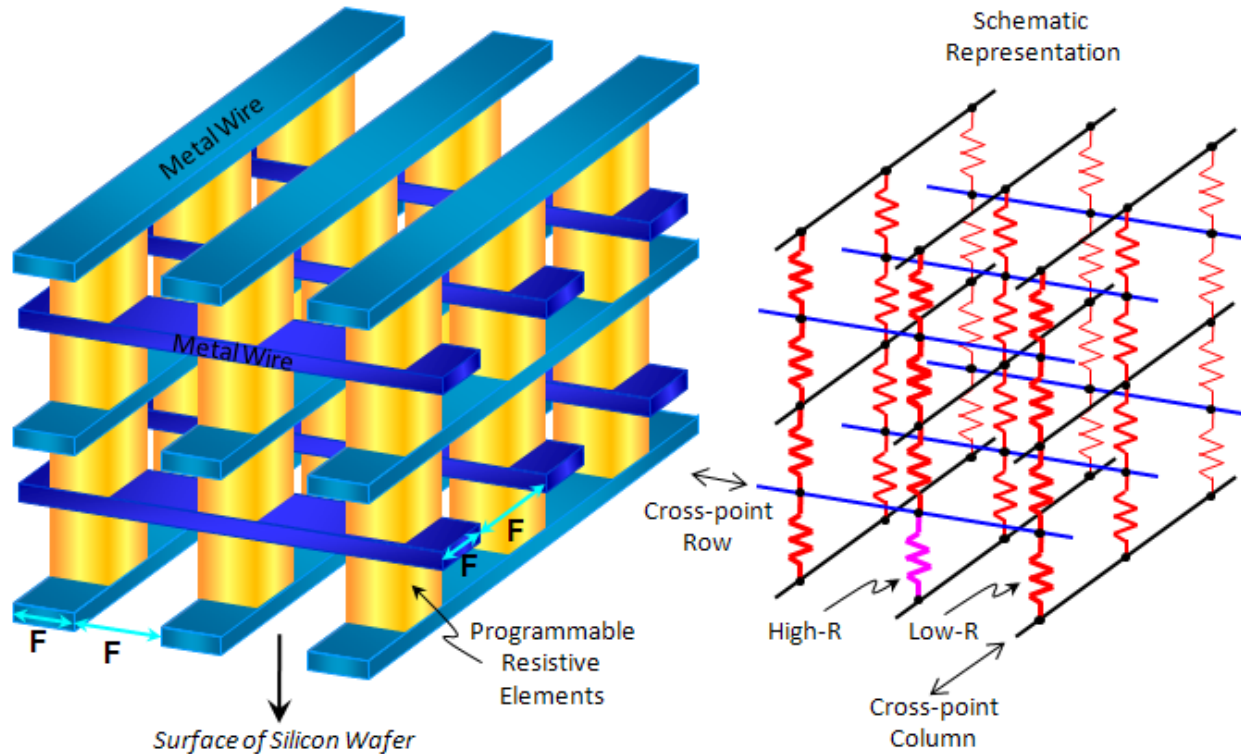
The use of a 3-terminal device for a storage element provides a very effective means for building large arrays of memory cells where a small sub-group of cells can be accessed without seeing an adverse interaction with the nearby cells which are not being accessed. In a two dimensional array of cells, the gate terminal of the 3-terminal devices can be connected in the “row” direction while the drain and source terminals can be connected in the “column” direction. Applying a moderate “turn-on” voltage to the gate terminal of the devices in a “selected” row causes all the devices in that row to connect to their respective column in the moderate resistance state. Applying a high “turn-on” voltage to all the other “non-selected” rows connects those devices to the respective columns in the “low” resistance state. In this biasing condition the total resistance along a column is dominated by the device on the selected row. Thus the programmed state or “data” of the device in the selected row can be determined by measuring the total resistance along the column. The minimum area in the silicon wafer needed to fabricate one device (or bit) is determined by the minimum feature dimension “F” of the technology.



The difficulty with this approach for building very high density memory devices is that the fabrication of the MOS Field-Effect Transistor is limited to the surface of the bulk silicon wafer. This limits the design of the memory device to only the base CMOS layers and thus to the 2-dimensional array just described. In contrast, new technologies have been developed which allow 2-terminal resistive elements to be fabricated in the metal/insulator layers that sit above the bulk CMOS layers. The value of the element's resistance can be modified by applying specific voltages across the element, thus allowing these elements to be used to store data in a manner similar to the Floating-Gate MOSFET described above. This opens the possibility of designing memory devices with multiple layers of memory arrays built one on top of another, giving us a 3-dimensional memory array which increases the number of bits of data which can be stored in a given amount of chip area by the number of memory layers that can be stacked vertically.

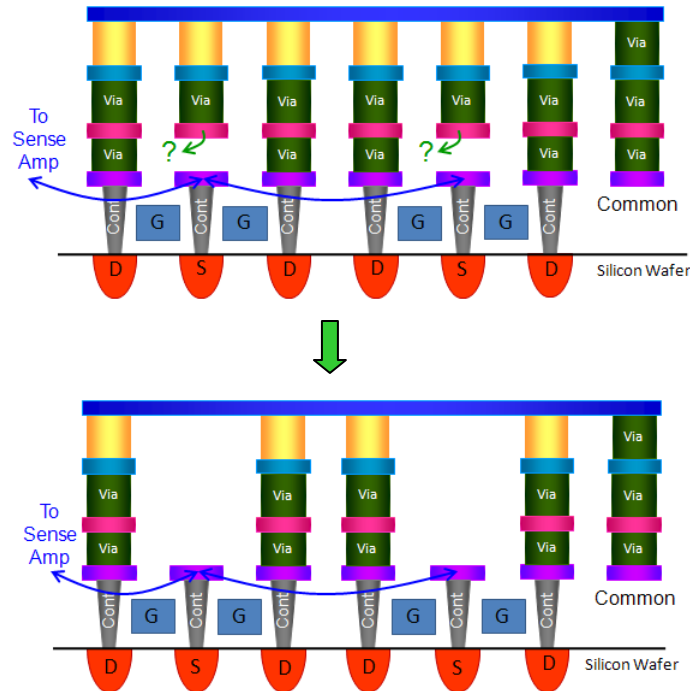


In these stacked arrays of 2-terminal resistive elements, the highest density is achieved when the devices are connected in what is called a cross-point memory array. This means that 2-terminal elements are placed between two grids of wires where one grid has the wires running left-to-right in the X-direction (rows) and the other grid has the wires running front-to-back in the Y-direction (columns). A 2-terminal resistive element is placed at each intersection of an X and Y wire with one terminal connected to the X-wire and the other terminal connected to the Y-wire. This creates a resistive current path between the X and Y wires at each intersection. Theoretically, the value of the resistor at any intersection can be measured by applying a voltage between a particular row and a particular column and then measuring the current that flows between the two.



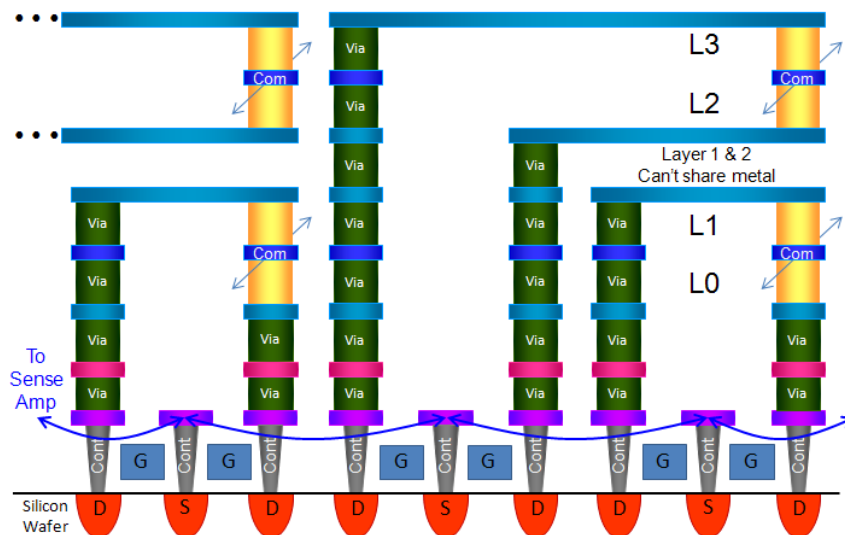
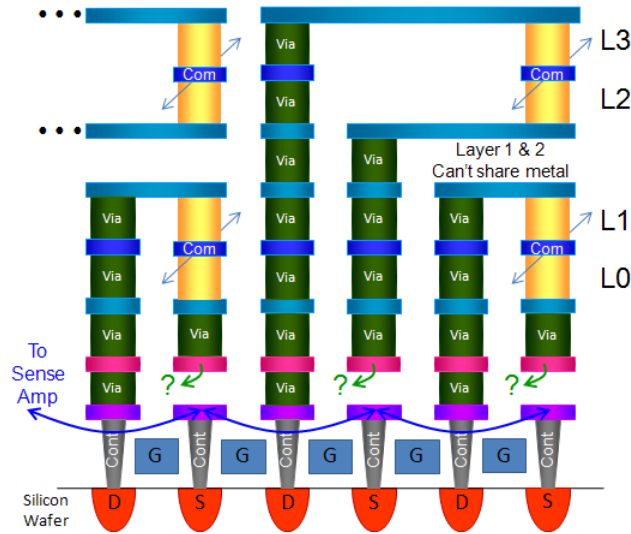
Unfortunately, with the absence of a 3rd control-gate terminal like those of the MOSFET device described above, the remaining elements along the row and column are not isolated from the selected element. This means that the voltage applied to the selected row and column causes some amount of current to flow through the other elements along both the row and column. These stray currents add to or subtract from the current flowing through the selected element at the cross-point, making it very difficult to precisely determine the programmed resistance of the “selected” element. This problem generally forces a memory design using these 2-terminal elements fabricated in the upper metal layers to connect each resistor element to a MOSFET device in the underlying bulk CMOS layers. This configuration is referred to as a 1T-1R array. The MOSFET is used as a selection device to prevent current from flowing through the un-selected elements when a voltage is applied between the row and column. However, for even a simple 1-layer array of resistor elements in the upper metals it is not possible to connect all of the resistor elements to underlying MOSFETs in the minimum pitch of the resistors (even if the MOSFETs have the same feature dimension “F” as the resistor elements) because

every third diffusion connection from the MOSFETs must connect to a common wire going the sensing circuitry. This leaves at least one third of the resistor elements unconnected.



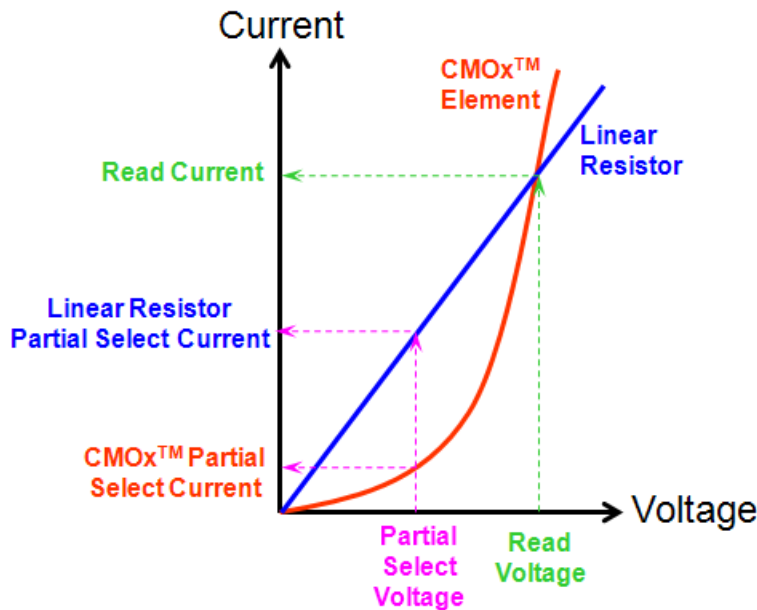
To connect all the resistor elements to MOSFETs, the resistor element spacing in the Source-to-Drain direction of the MOSFETs must be increased to where the resistor elements match up with each drain terminal of the MOSFETs. This increases the size of the resistor element array in the Source-to-Drain direction of the MOSFETs by at least 33%. And this doesn't even address how the common wire from the sensing circuitry can be routed around the contacts connecting the resistor elements to the MOSFET drain terminals in order to get to the contacts connecting to the MOSFET source terminals.

This problem gets even worse when we start adding additional layers of resistor element to this 1T-1R array. To connect a MOSFET terminal to a resistor element in an upper layer, a gap must be inserted between resistor elements in the lower layers to accommodate the vias that form the vertical connection. As more layers are added, more gaps are required. These gaps require as much space as the resistor elements they push aside and thus spread out the individual 2-terminal resistor elements over a much greater area, further negating the advantage of stacking these layers vertically.

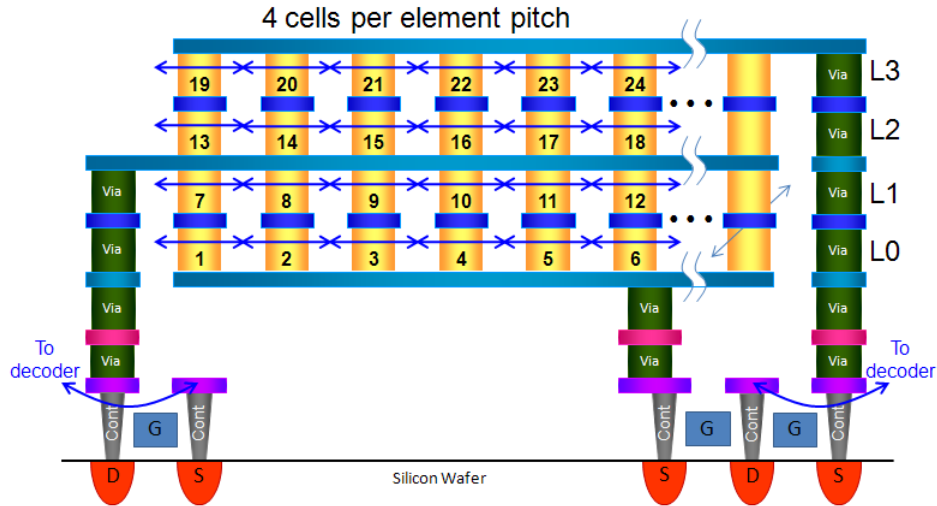


And after the gaps for the vias are inserted, we still have the same problem of every MOSFET source terminal having to be connected to the wire routing to the sense circuitry. So as with the 1-layer example, the resistor elements and vertical stacks of vias must be spread out to line up with the MOSFET drain terminals which increases the size of the resistor array even further. What you finally see here is that adding additional layers of resistor elements does not increase the density of the array because the array size is limited by the MOSFET elements in the underlying CMOS wafer – 1 MOSFET for every resistor element. Furthermore, the density of the MOSFETs is actually less than that of the NAND-Flash array described above because all the MOSFETs in the NAND-Flash array can share both their drain and source terminal with the adjacent MOSFET while in this 1T-1R array the MOSFET drain terminals cannot be shared.

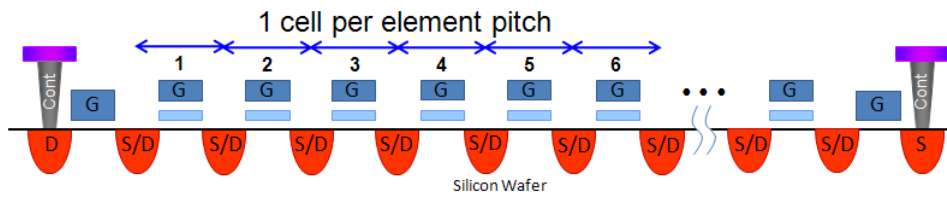
As can be seen, the need to electrically isolate the 2-terminal elements in some manner to prevent or reduce stray currents presents a major obstacle to the ability to fabricate either a single-layer or multi-layer cross-point memory array. However, Unity's CMOx™ memory technology eliminates the need for such an isolation device because the current vs. voltage behavior of the CMOx™ element is non-linear. This means that the resistance value of the CMOx™ memory element decreases as the voltage applied to the element increases.



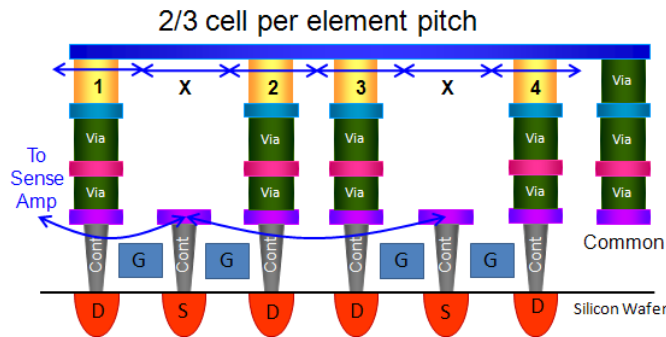
(This is not to be confused with the programming/erasing attributes of the CMOx™ element which allows the resistance value of the element at a specific applied voltage to be increased or decreased by applying a larger programming or erasing voltage to the element.) At small values of applied voltage the resistance of the element is extremely high, allowing very little current to flow thru the element. As the applied voltage increases, the resistance of the element decreases, allowing the current flowing through the element to increase by a larger percentage than the change in the applied voltage. This enables the functionality of a true cross-point array of CMOx™ elements because the unwanted stray currents that flow through the un-selected elements along the column, which see only a small applied voltage, are dramatically reduced which makes it possible to accurately determine the resistance of the CMOx™ element located at the cross-point of the selected row and column. With the isolation problem solved, the CMOx™ cross-point memory array does not require a dense array of MOSFET transistor under the cross-point array to provide isolation. The only MOSFET elements required are for connections near the edge of the array to the individual row and column wires of the cross-point array which means that the memory bit density of the array is limited by the minimum density of the resistor elements and not by the MOSFET devices that connect to them.



CMOx™ Cross-point Memory Array



NAND Flash Memory Array



1T-1R Resistor Element Memory Array

In conclusion, the unique electrical properties of CMOx™ memory technology enable the building of true cross-point memory arrays and the stacking of these arrays vertically to achieve dramatically higher memory densities than that offered by conventional NAND Flash technology or by that offered by other proposed resistor-element memory technologies.