



— UNITY SEMICONDUCTOR —

Scalable Non-Volatile Cross-Point Memory
based on
Dual-Layer Oxide Memory Elements

Rene Meyer

rmeyer@unitysemi.com

Unity Semiconductor Corporation
255 Santa Ana Court, Sunnyvale, CA 94085

9th Annual Non-Volatile Memory Technology Symposium, November 11-14, 2008, Pacific Grove, CA

Co-authors

- Wayne Kinney
- Larry Schloss
- Roy Lambertson
- Julie Brewer
- John Sanchez
- Darrell Rinerson
- Unity Semiconductor staff



Outline

- Unity
 - technology approach
- Unity memory cell
 - structure
 - scaling
 - underlying physics
 - comparison to binary oxides
- Summary



How to beat Flash ?

Flash Cell Scaling Limits

Year	2004	2006	2008	2011	2014
Node	90nm	65nm	45nm	32nm	22nm
NOR					
NAND					

Main scaling issues:

- Tunnel oxide thickness
- Interpoly dielectric thickness
- Cell gate length
- Contact dimension/ isolation spacing
- Cell proximity (cross talk)

Enable Multiple Memory Layers



Challenges of a Physical Multilayer Memory Approach

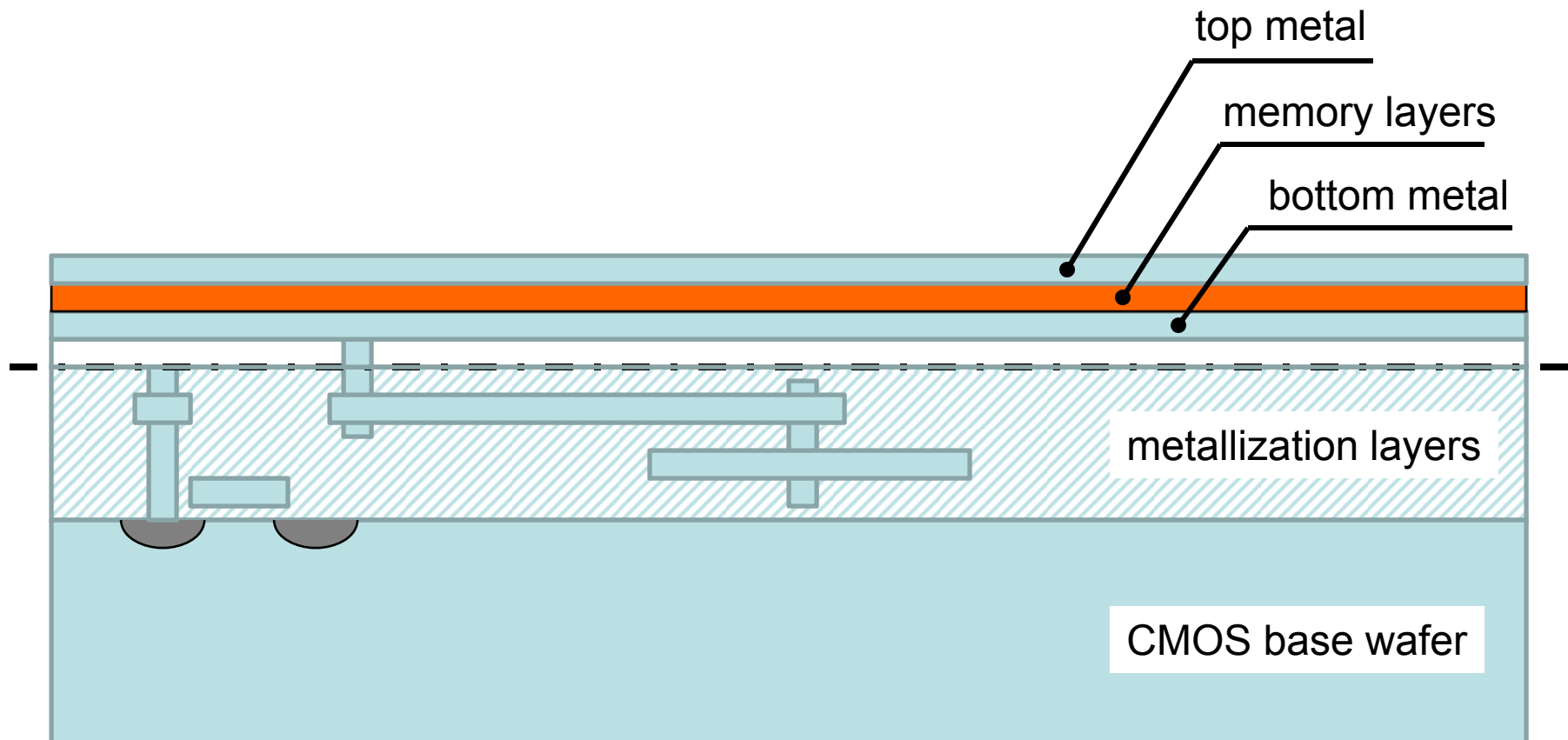
- We cannot utilize transistors as selection devices.
- However, a diode-like selection device is needed.
- No selection device is available that is compatible with a **high current** cell multilayer approach.
- **The memory cell current (both program and erase) has to scale with area!**



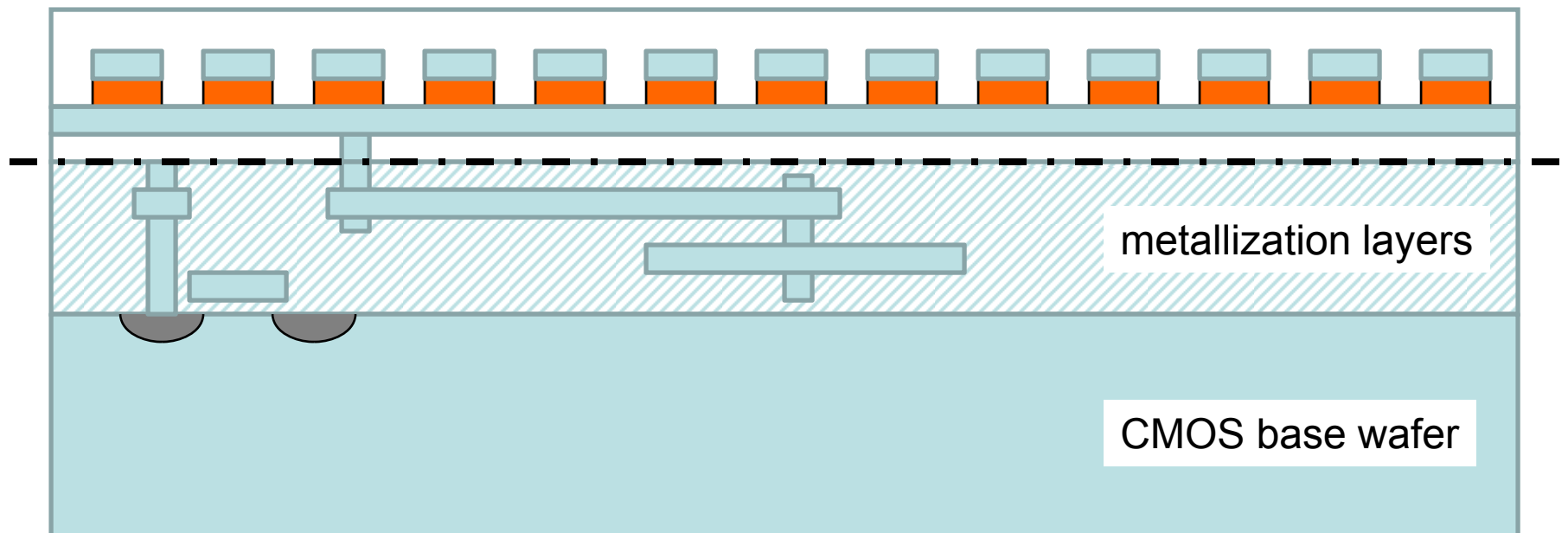
- Unity = CMOS compatible Multilayer **BEOL** approach using a *scalable* memory device.



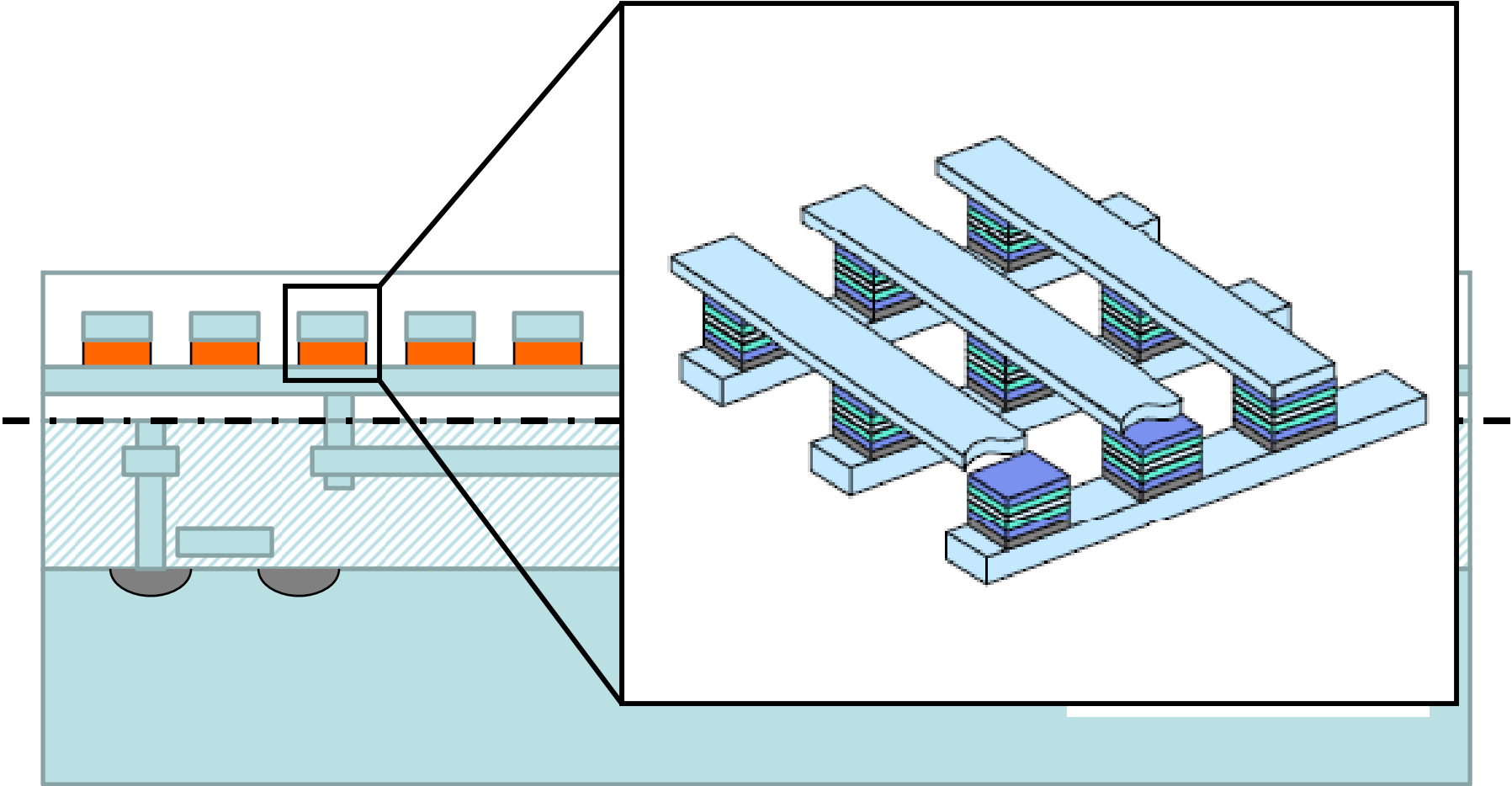
BEOL approach



BEOL approach



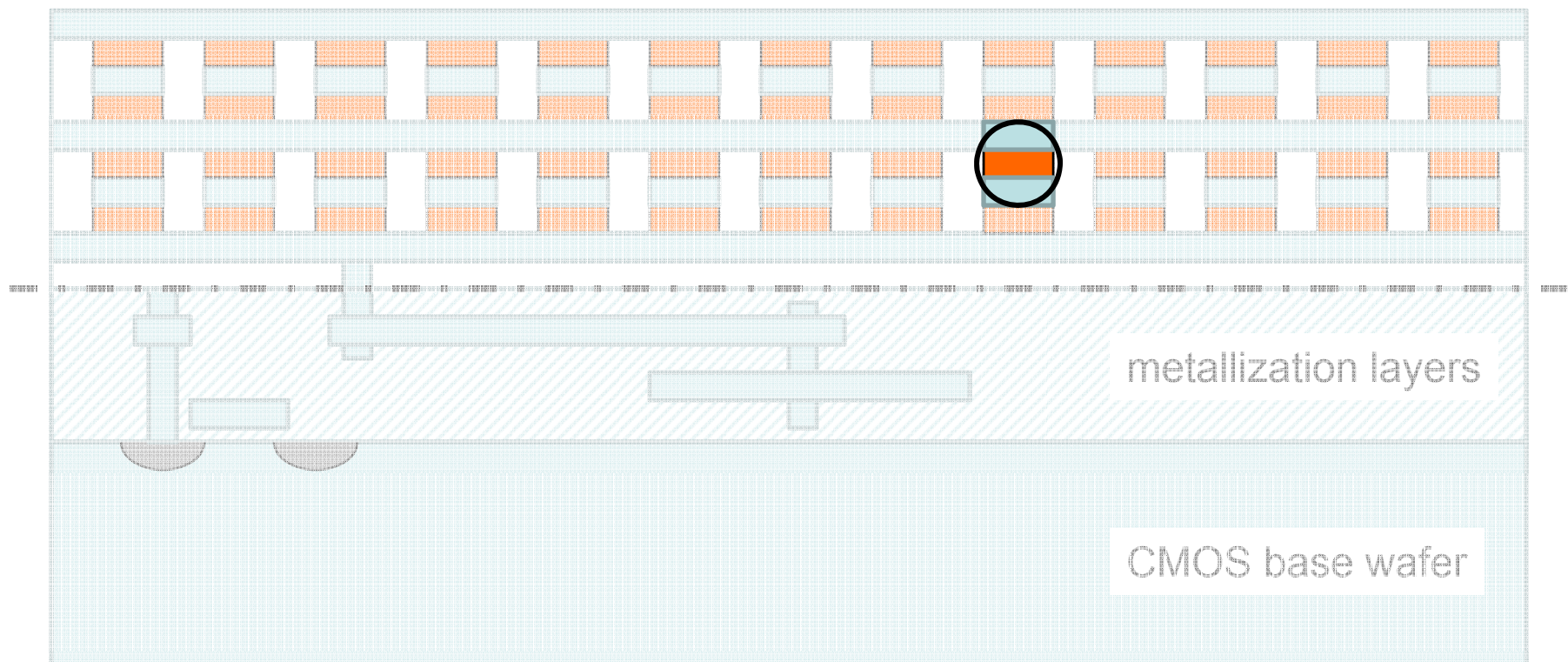
BEOL Transistorless Cross Point Memory Array



Multiple Physical Memory Layers

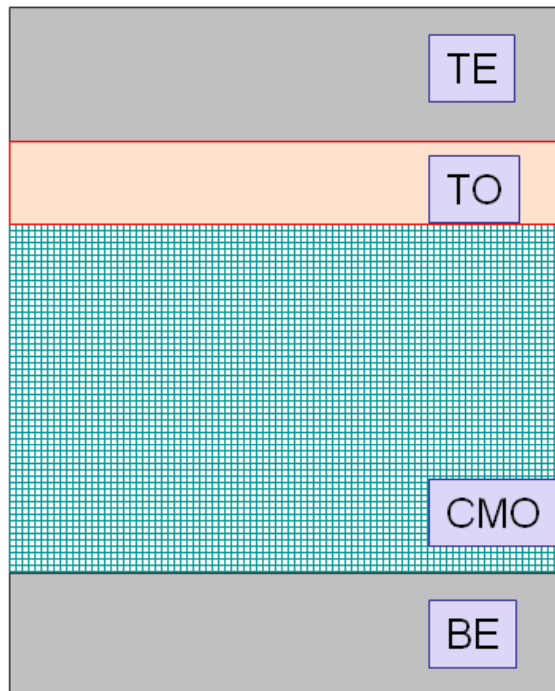
The front-end is conventional CMOS.

The new technology is in the back-end **memory cell** itself.



Unity memory cell

Memory Cell Structure

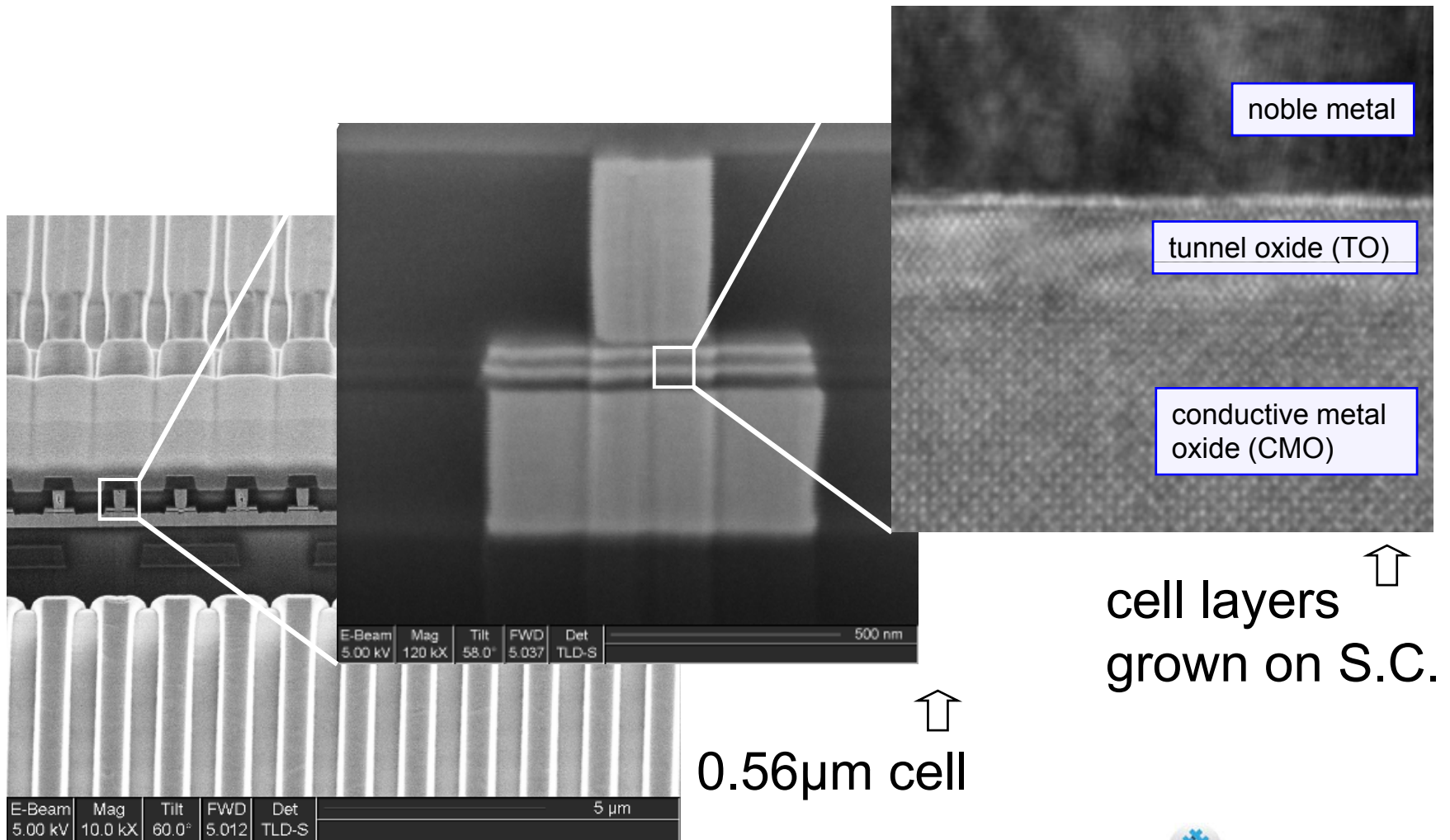


TE: Top Electrode (Pt)
TO: Tunnel Oxide 20-30Å
CMO: Conductive Metal Oxide
BE: Bottom Electrode (Pt)

Device current is determined by quantum mechanical tunneling (trap-assisted tunneling) through the **deposited** tunnel oxide.



Integrated memory cell



cell layers
grown on S.C.

0.56 μm cell



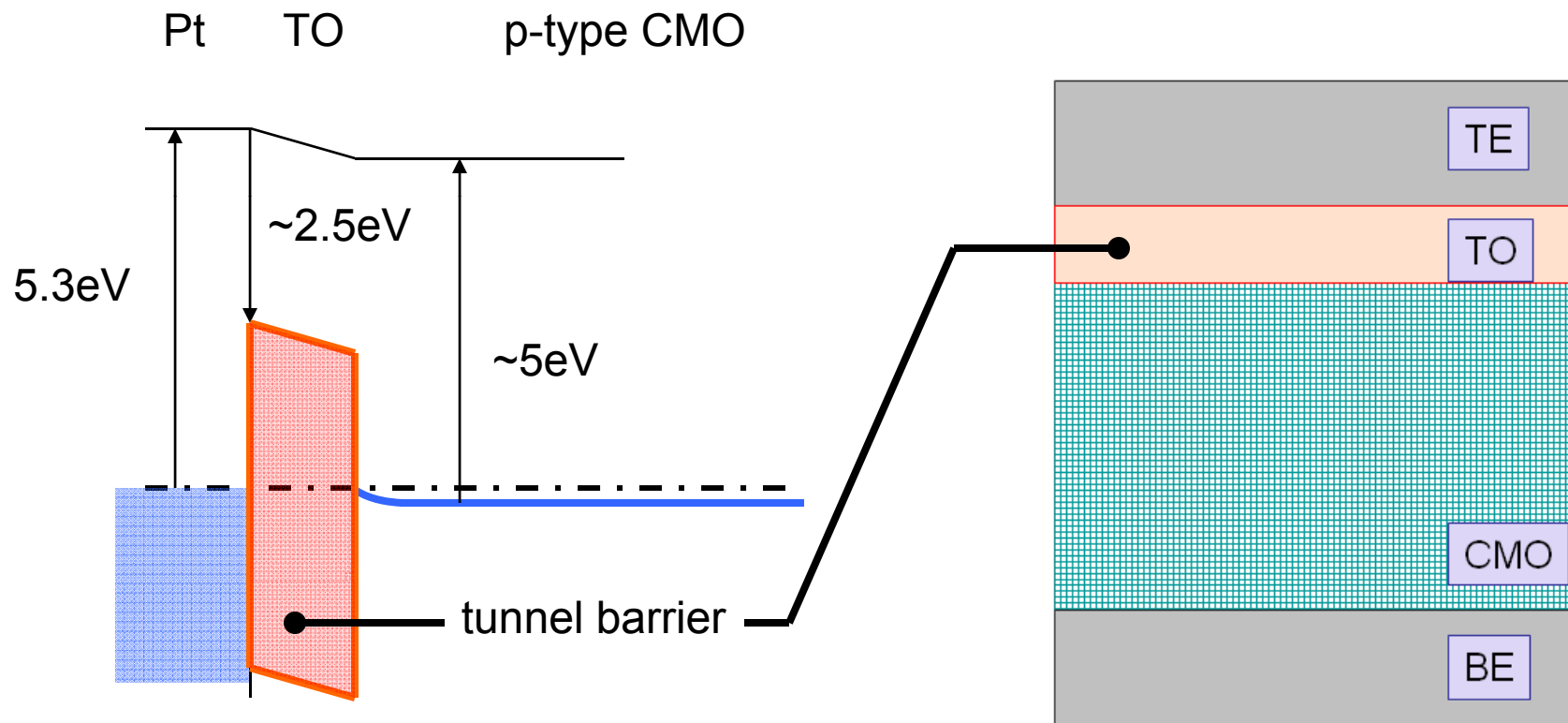
Electrical data

- *Effect of Tunnel barrier thickness
- I-V hysteresis (DC programming)
- *Device-to-device variations
- *Area scaling (un-programmed device)
- *Cycling without forming
- *Area scaling (program & erase state)

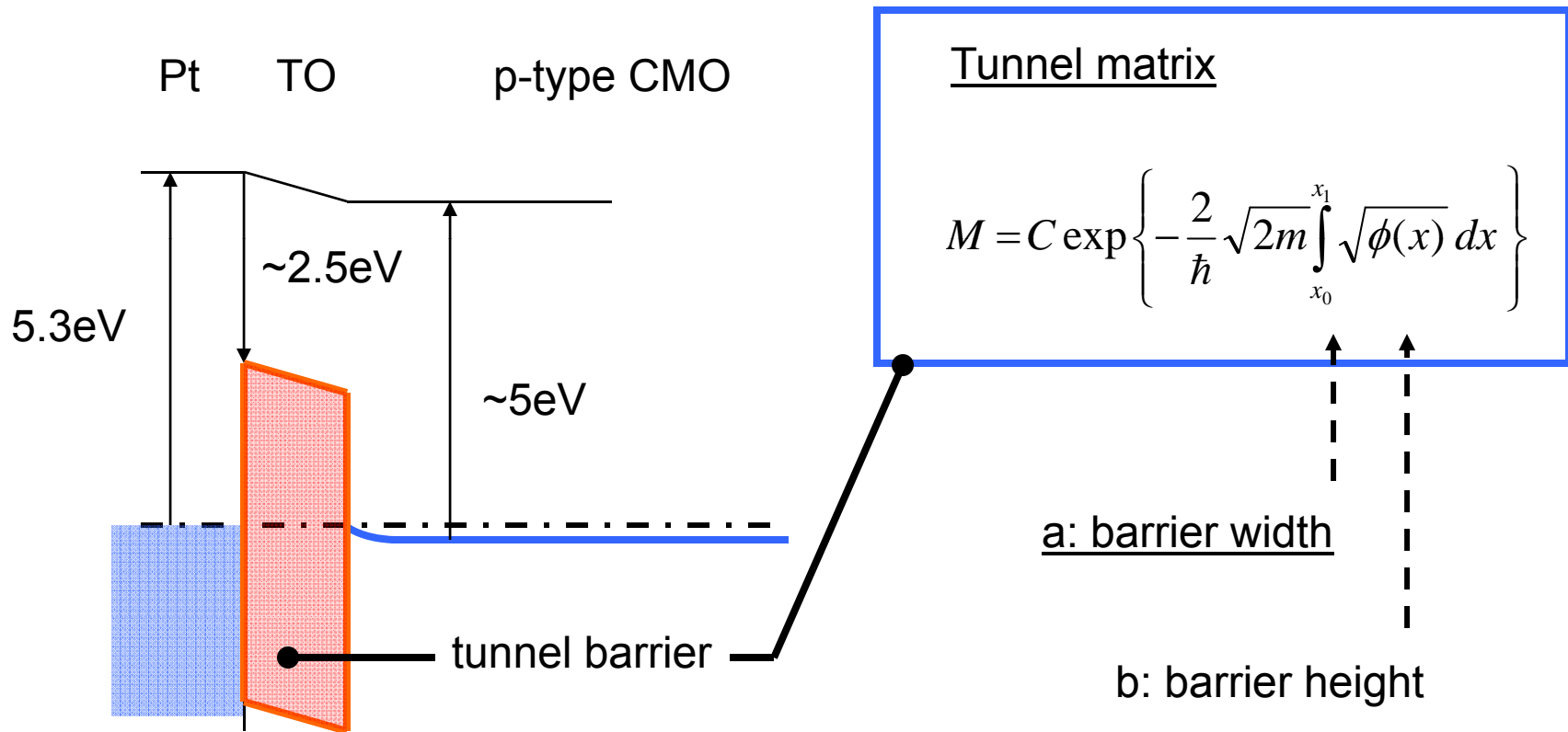
*Unity BEOL Memory Cell Requirements



Tunneling through a thin oxide



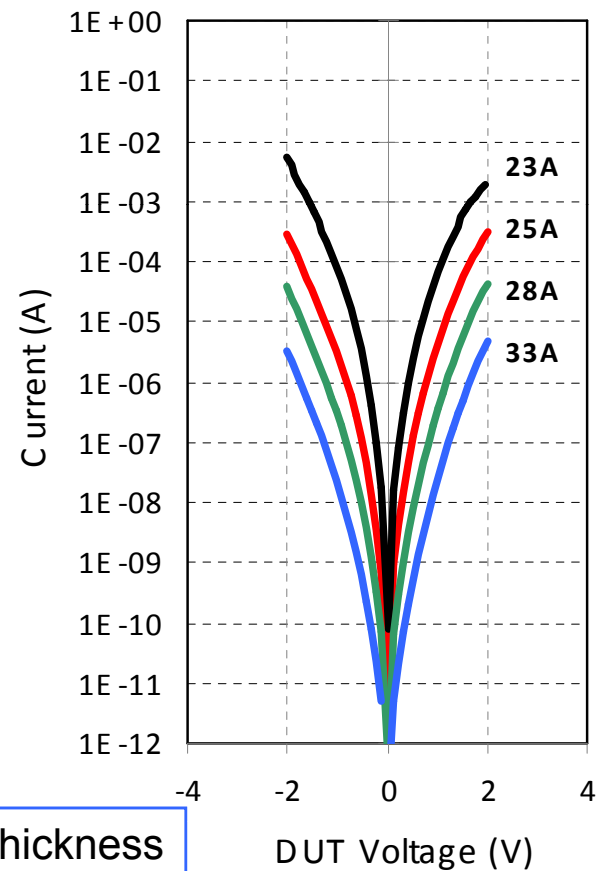
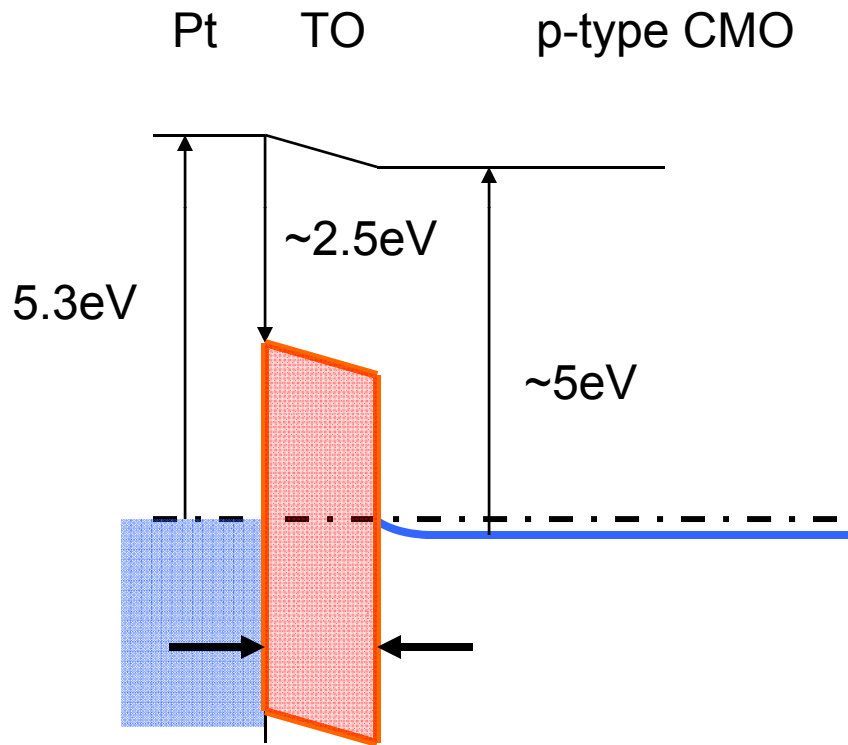
Tunnel matrix element determines tunnel current



Current depends exponentially on barrier thickness



Tunnel current for different barrier thicknesses

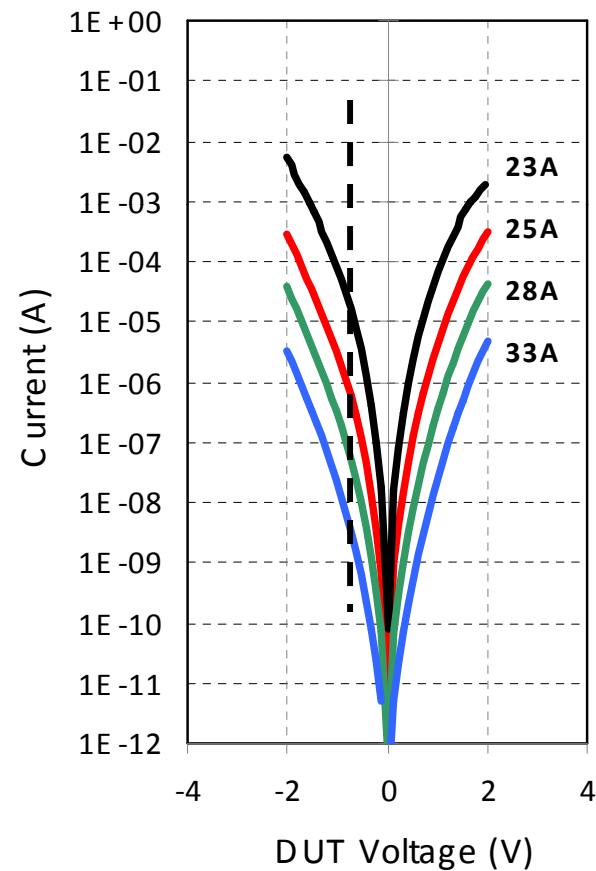
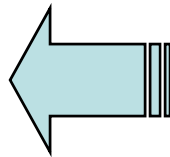
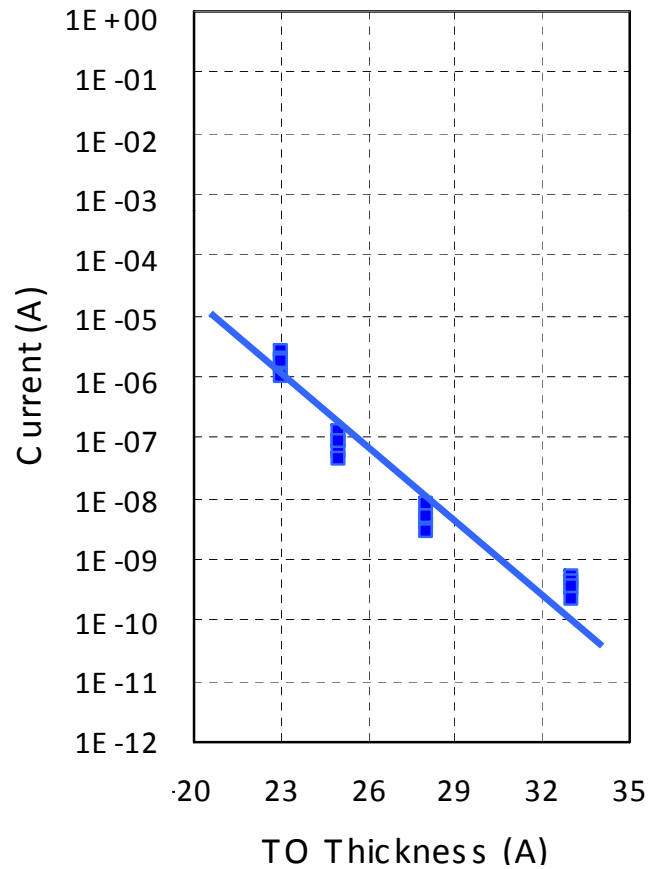


Current depends exponentially on barrier thickness

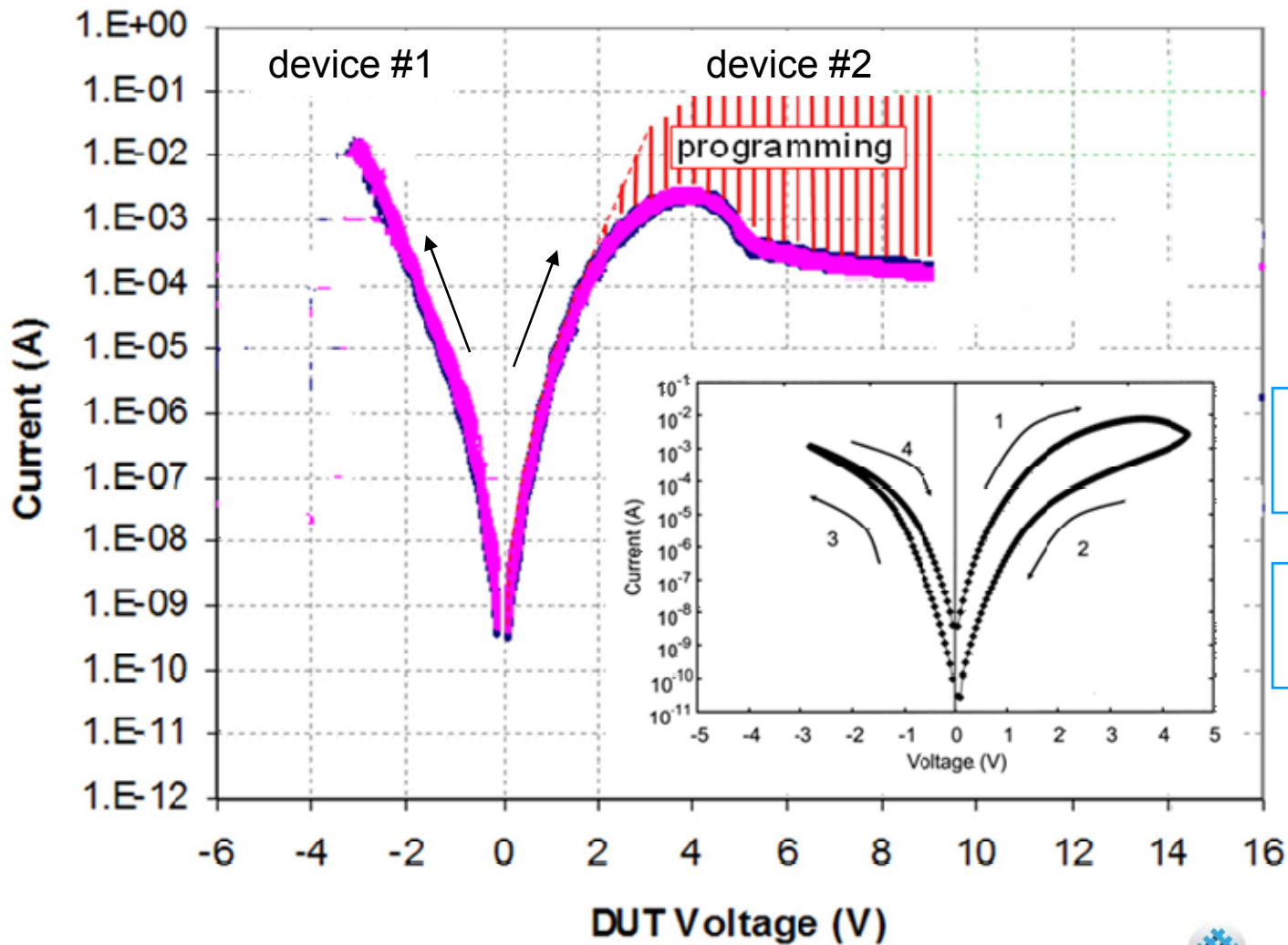


Tunnel current at a fixed read voltage

Tunnel barrier *width* allows us to **adjust current** for a given device area



DC programming and IV hysteresis at higher voltages

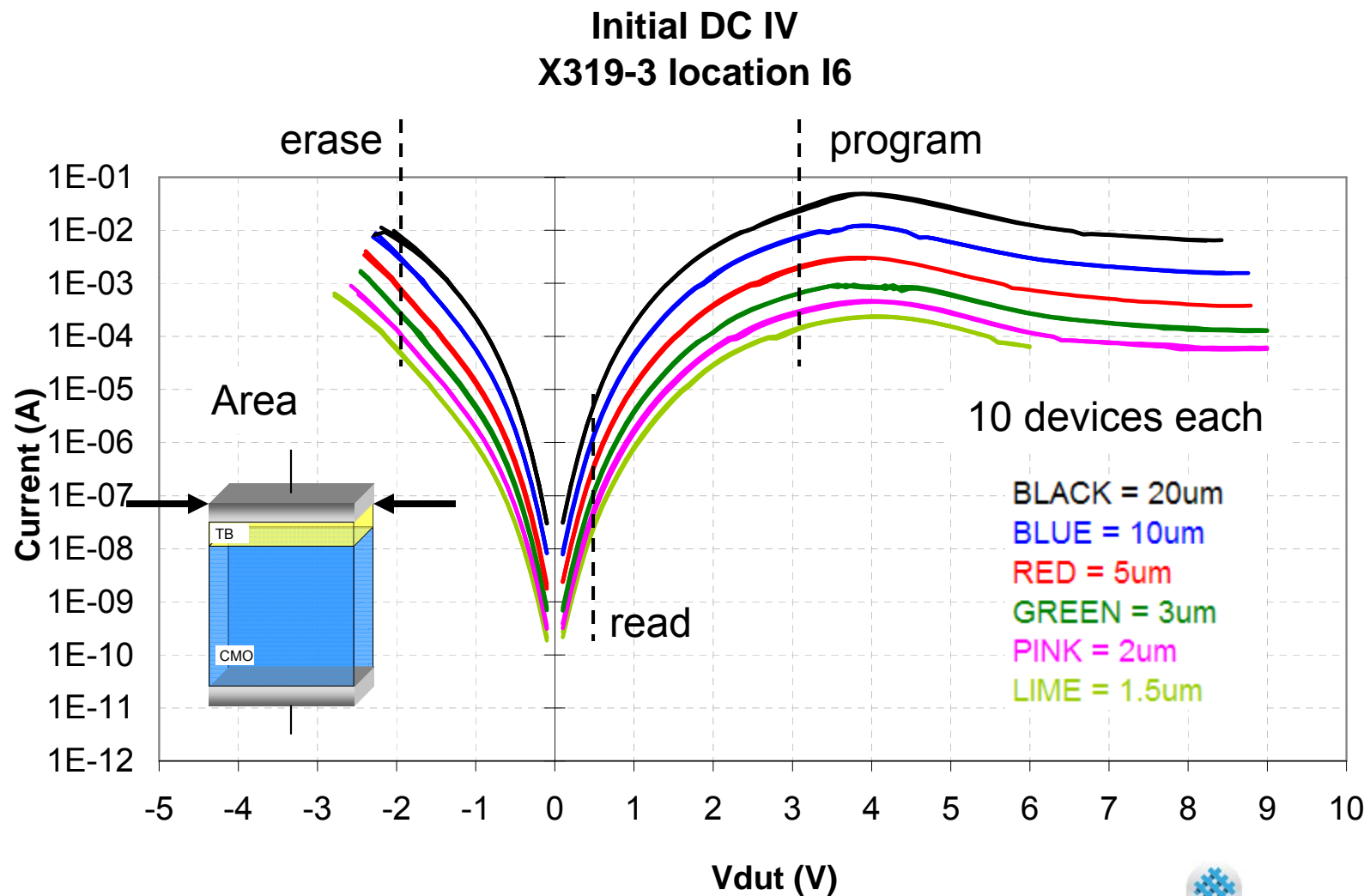


no program
"event"

no forming
needed

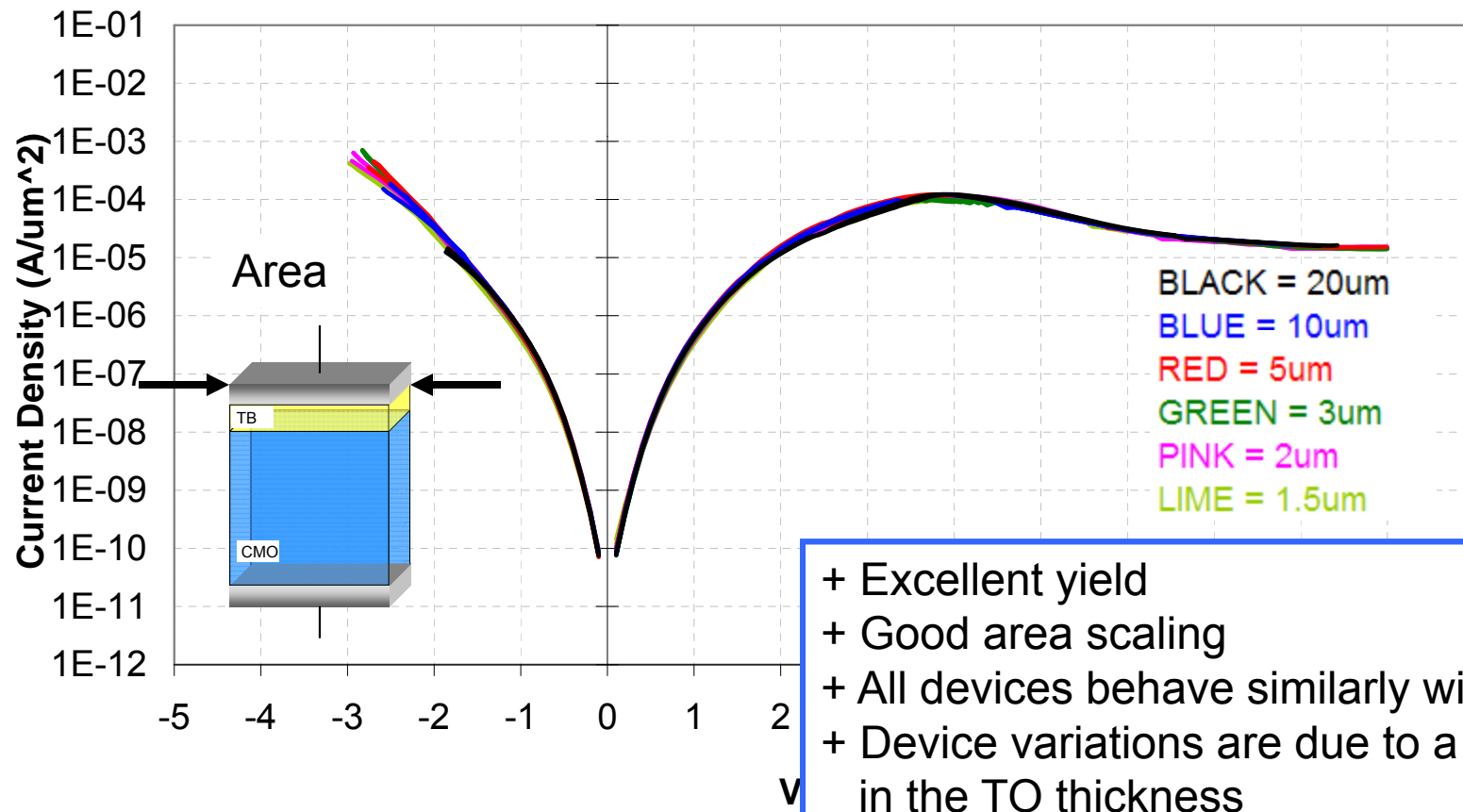


Uniformity and Repeatability I-V

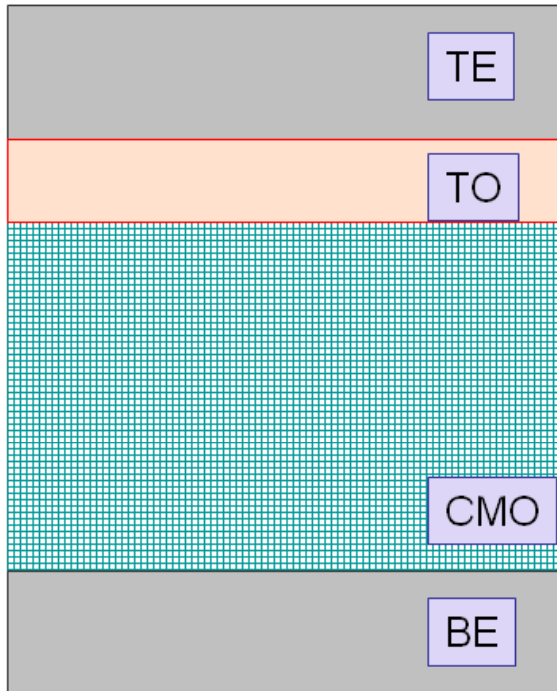


Uniformity and Repeatability J-V

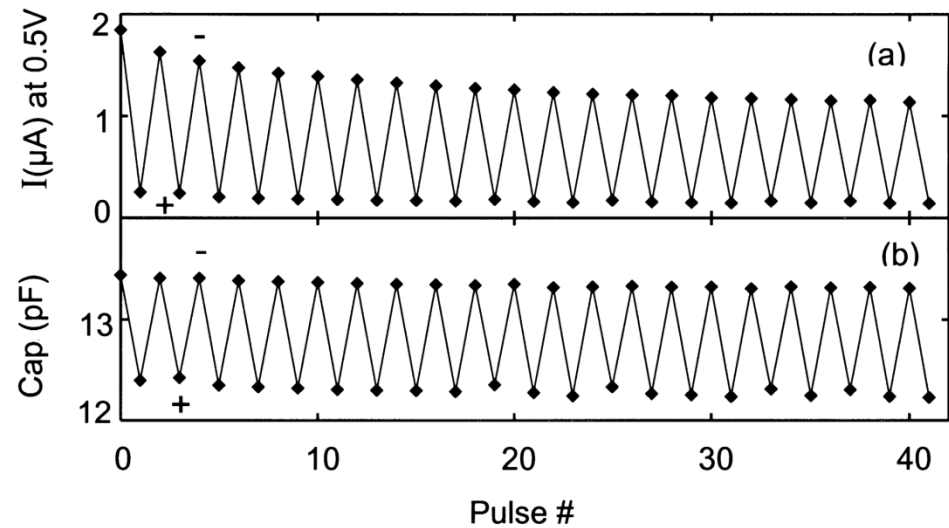
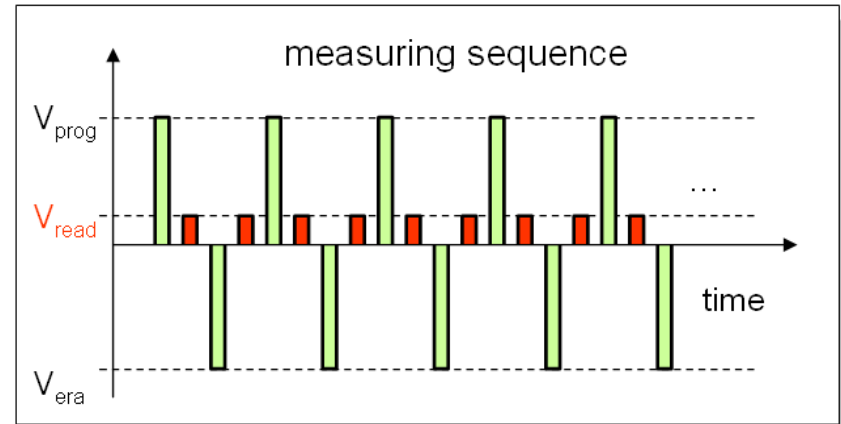
Initial DC JV
X319-3 location I6



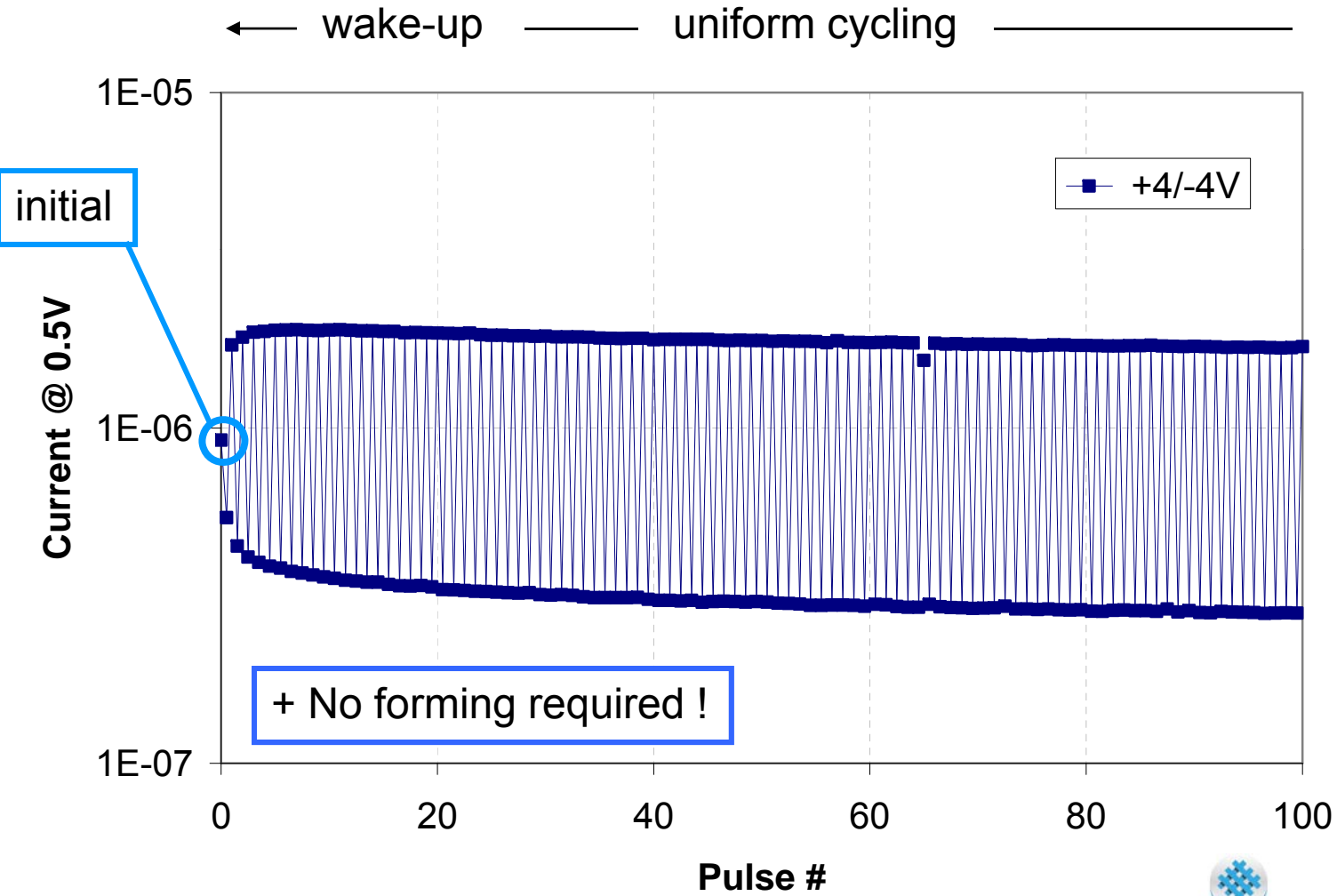
10x Current Change Cycling



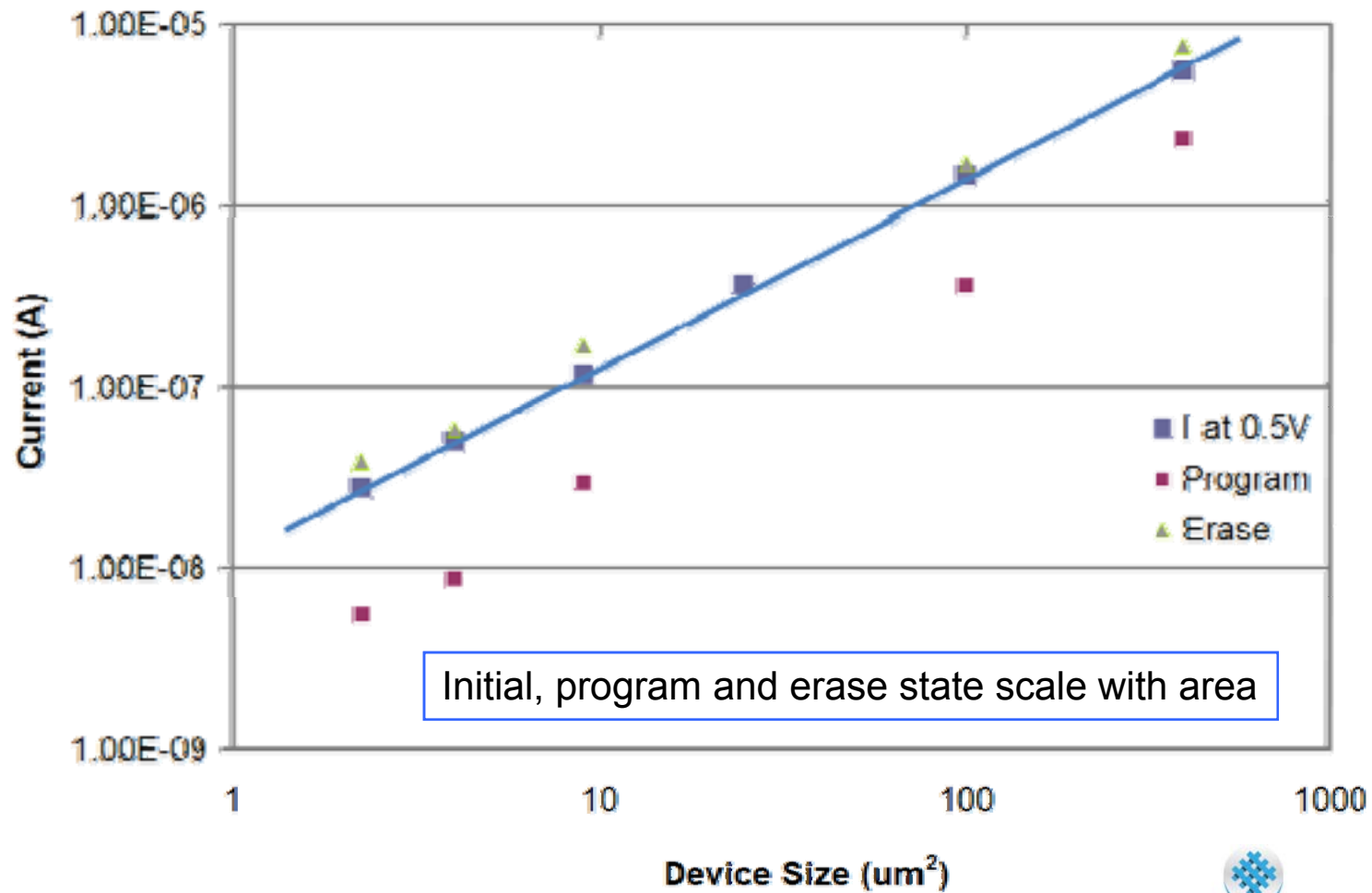
program/erase time: ~1 μ s
current change: 10x



Cycling behavior



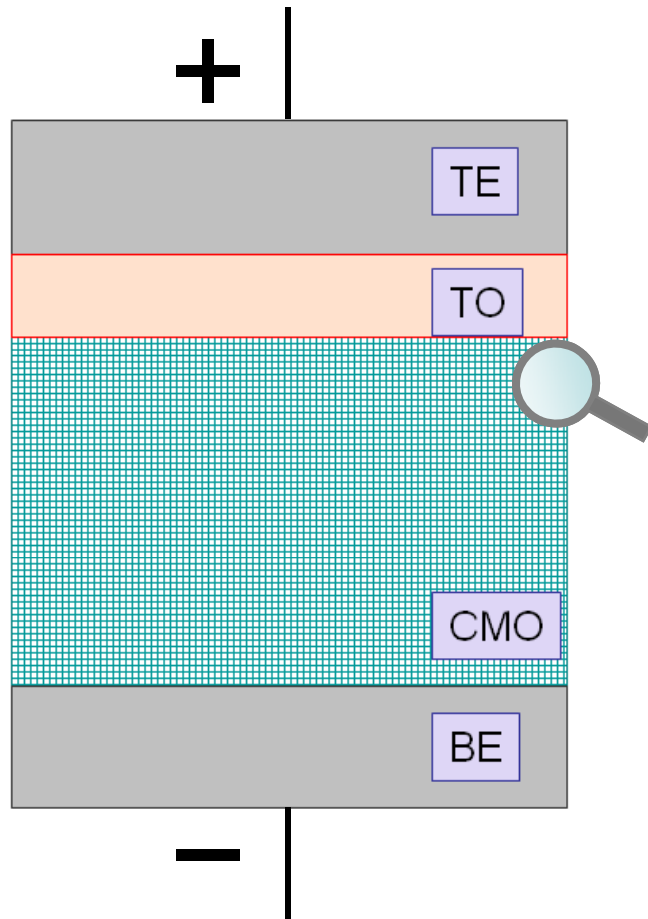
Area Scaling



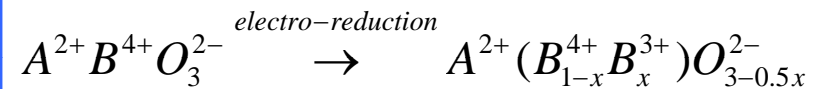
What is the memory effect?



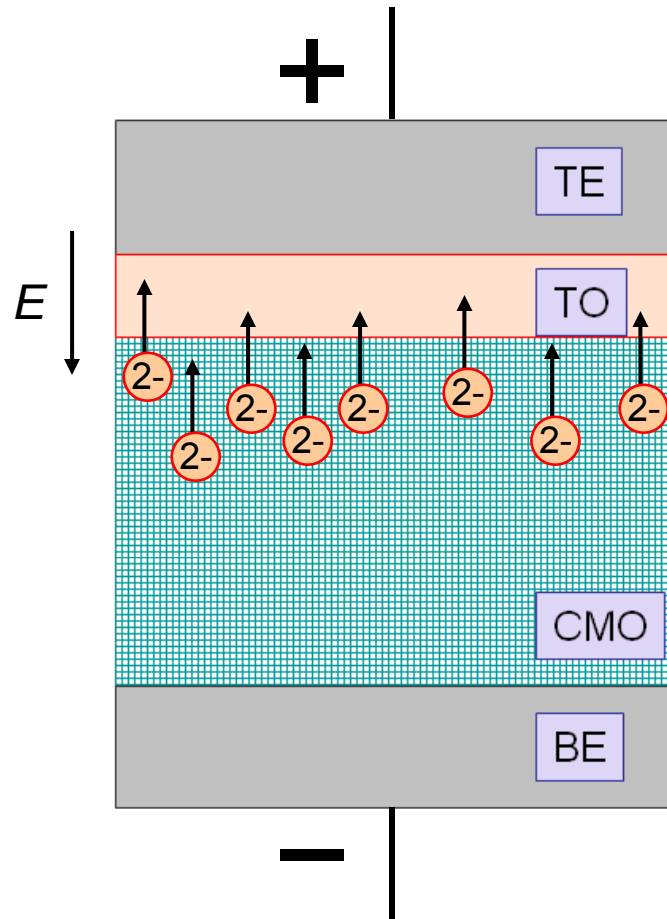
Memory Mechanism: Oxygen Redistribution



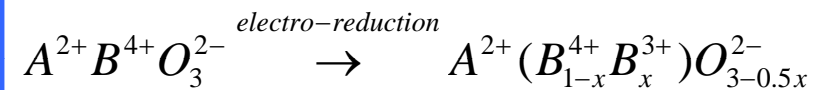
Valence change in the CMO indicates change in the oxygen stoichiometry (EELS):



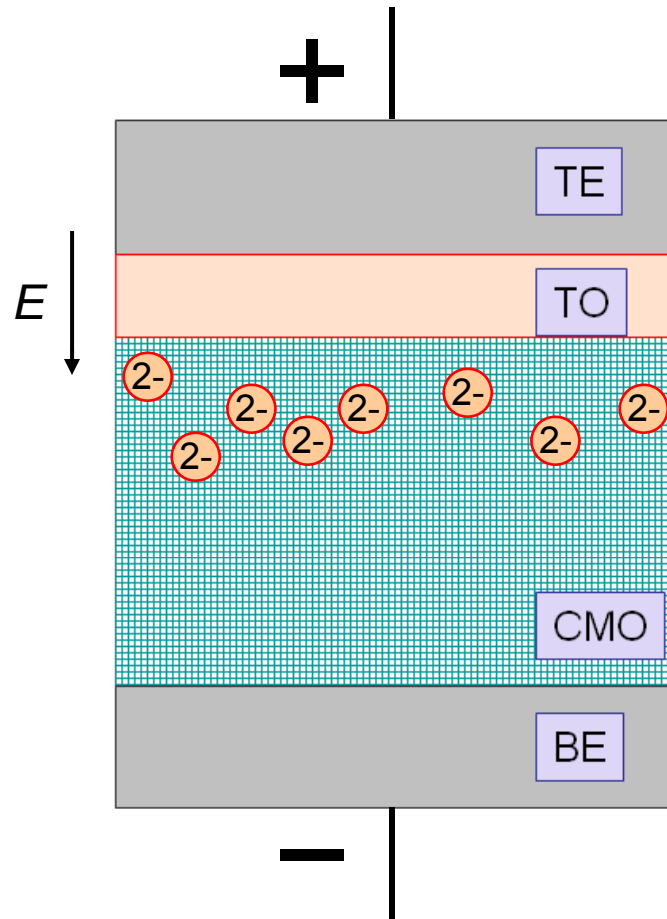
Memory Mechanism: Oxygen Redistribution



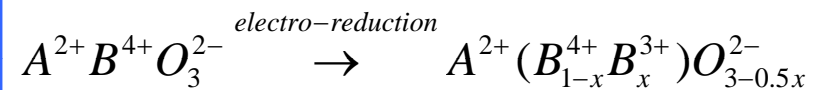
Valence change in the CMO indicates change in the oxygen stoichiometry (EELS):



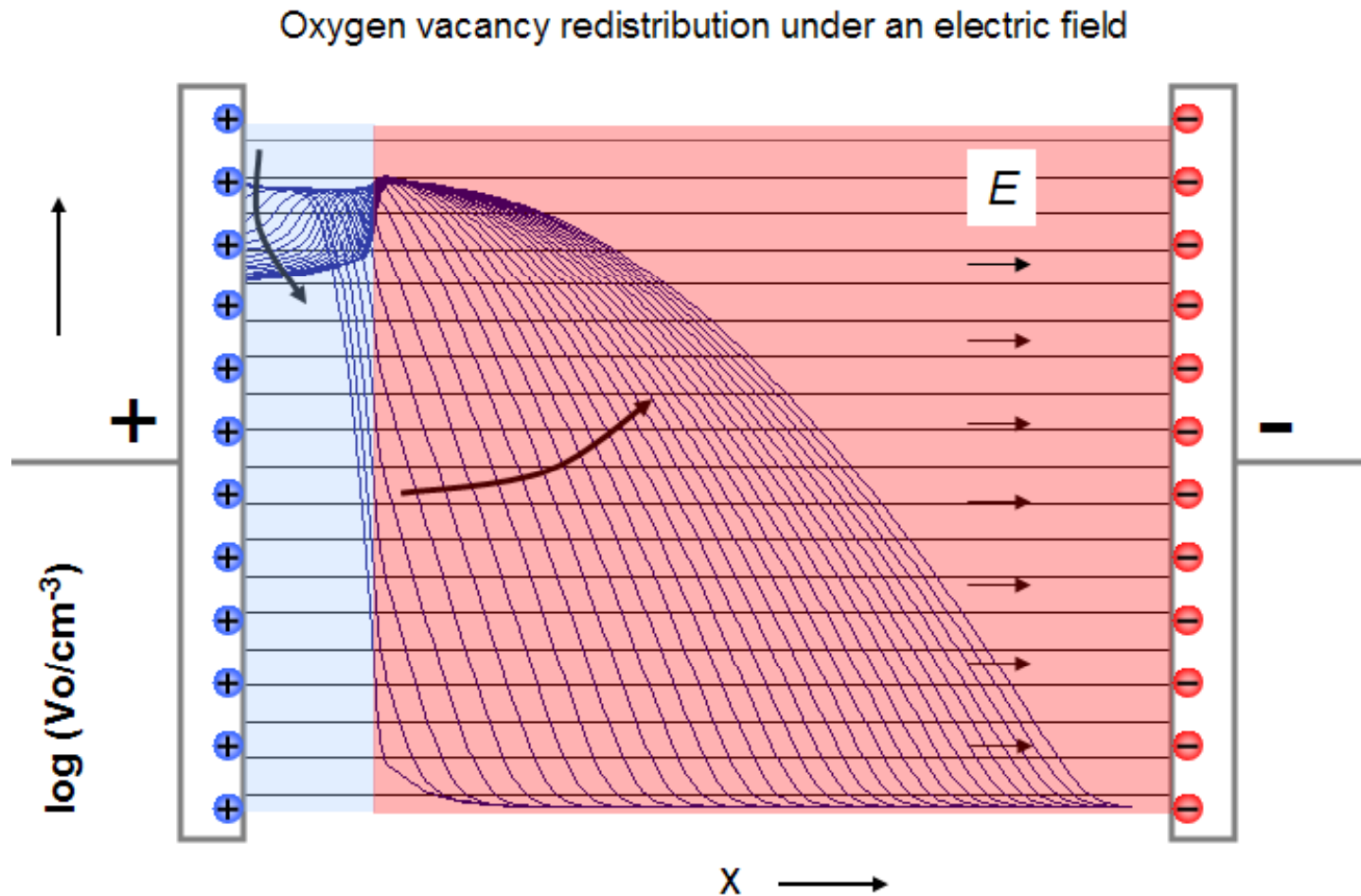
Memory Mechanism: Oxygen Redistribution



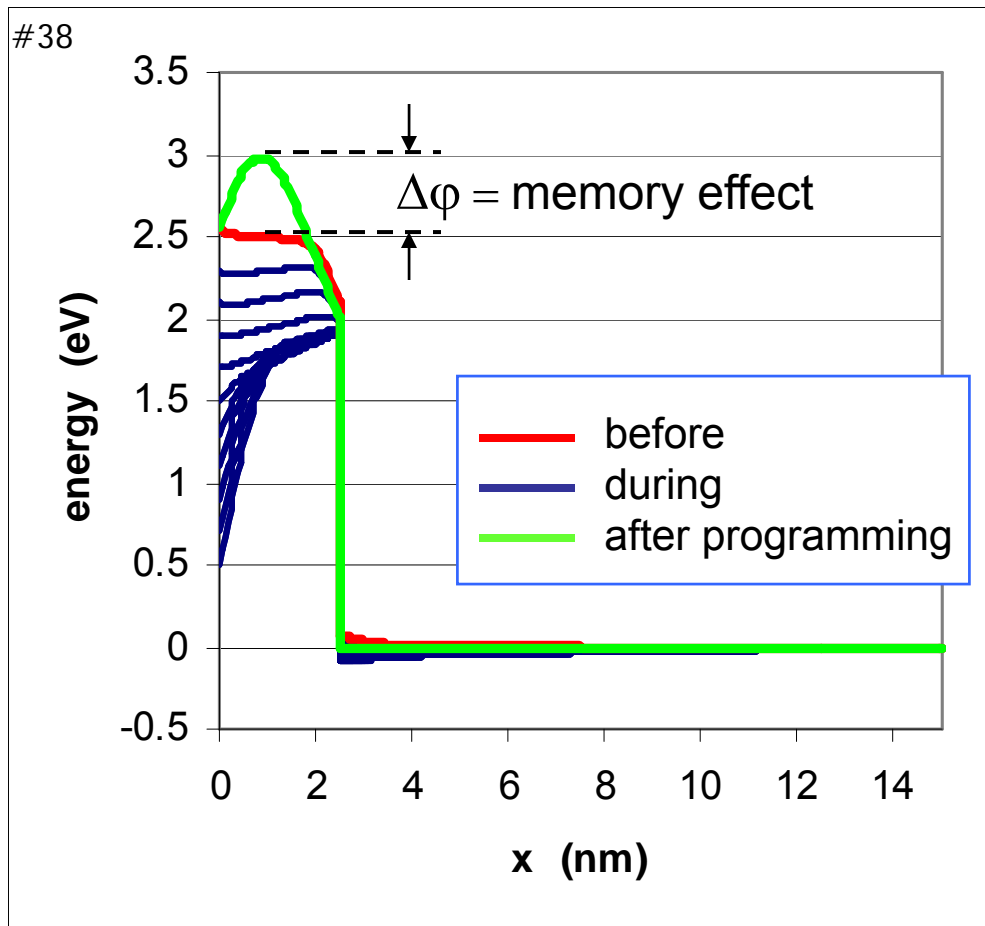
Valence change in the CMO indicates change in the oxygen stoichiometry (EELS):



Numerical model allows quantitative calculation of V_o redistribution under E-field



Change of potential barrier *height* after programming causes memory effect

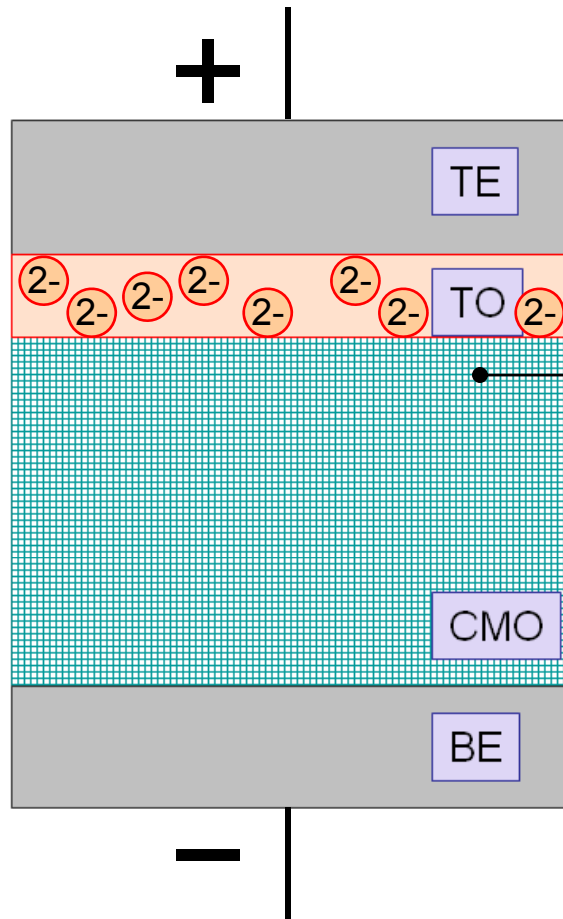


Results:

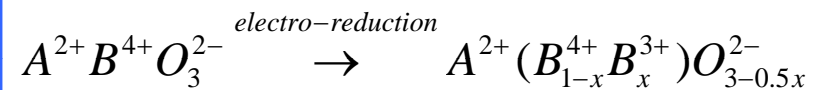
- Change of ϕ barrier height likely to cause memory effect.
- **The barrier height increase is caused by uncompensated charge in the TO.**



Memory Mechanism: Oxygen Redistribution



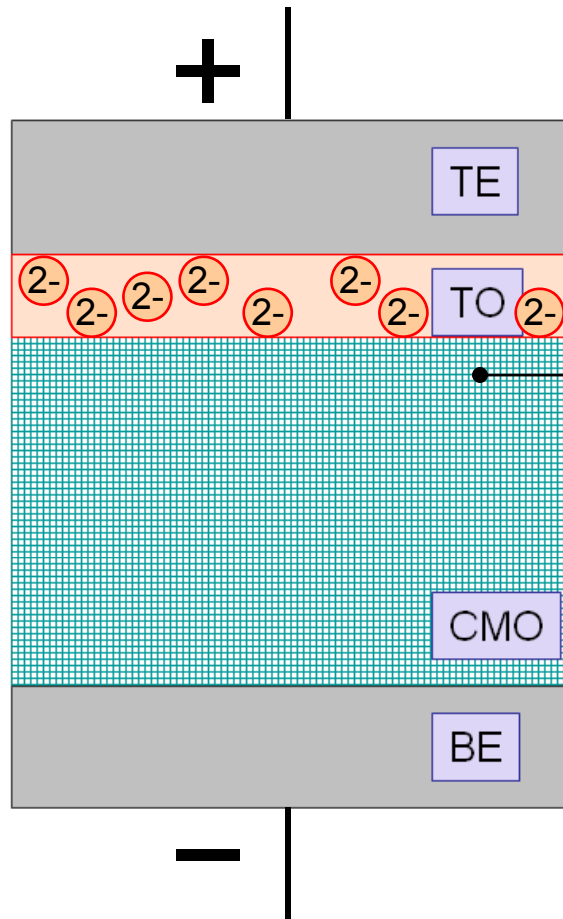
Valence change in the CMO indicates change in the oxygen stoichiometry (EELS):



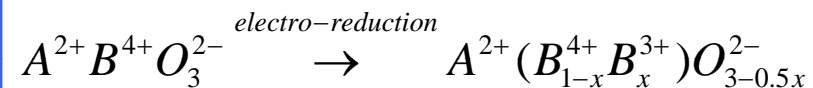
A negative charge build-up in the tunnel oxide reduces the tunnel current.



Memory Mechanism: Oxygen Redistribution



Valence change in the CMO indicates change in the oxygen stoichiometry (EELS):



A negative charge build-up in the tunnel oxide reduces the tunnel current.

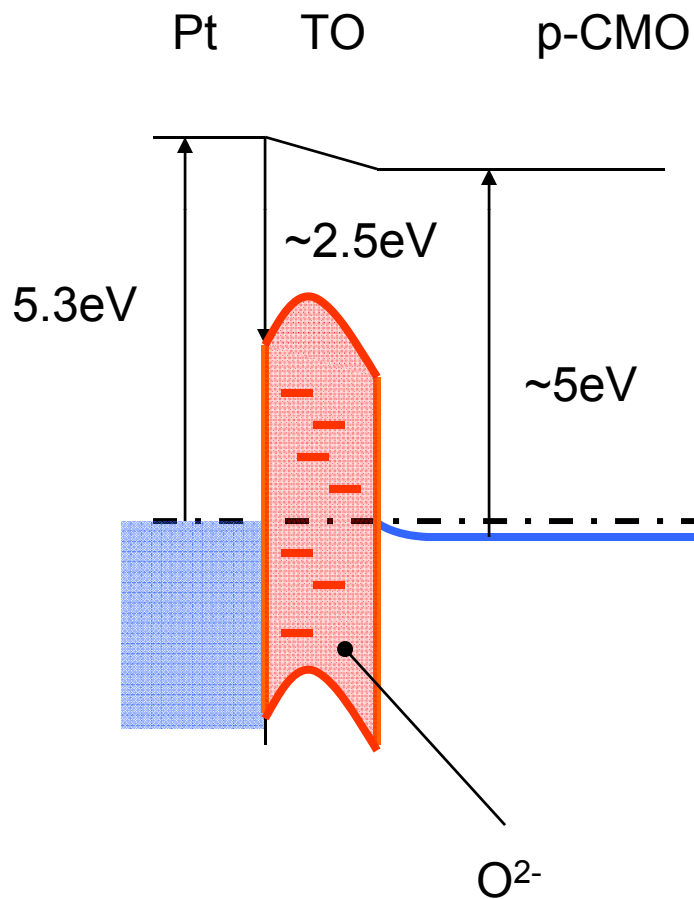
Tunnel matrix

Change of barrier height

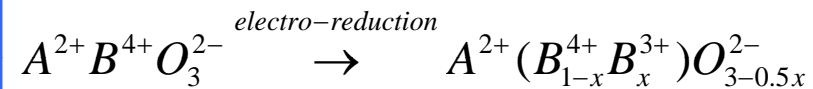
$$M = C \exp \left\{ -\frac{2}{\hbar} \sqrt{2m} \int_{x_0}^{x_1} \sqrt{\phi(x)} dx \right\}$$



Function of the Tunnel Barrier II



Valence change in the CMO indicates change in the oxygen stoichiometry (EELS):



A negative charge build-up in the tunnel oxide reduces the tunnel current.

Tunnel matrix

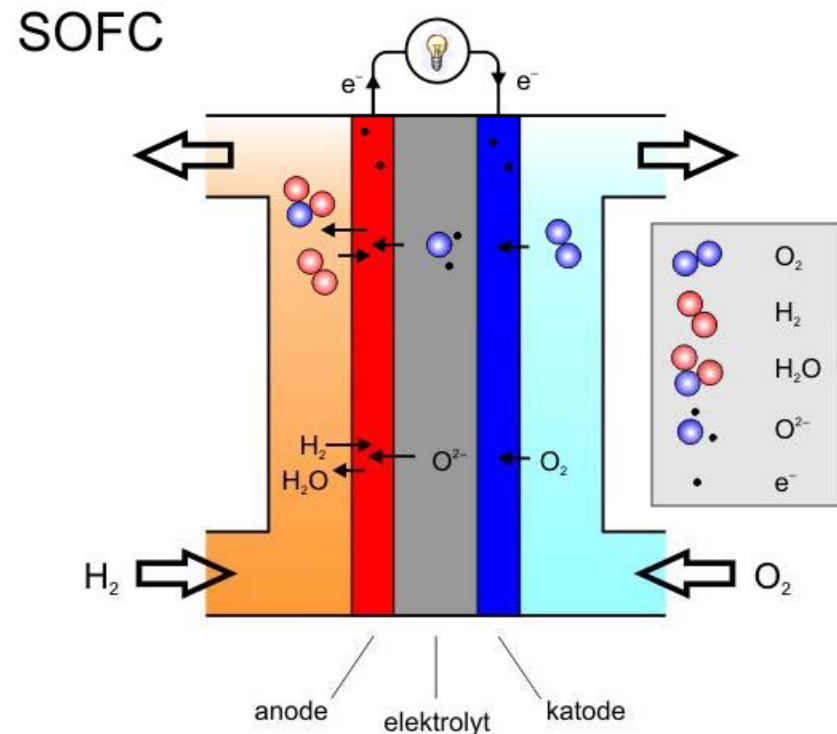
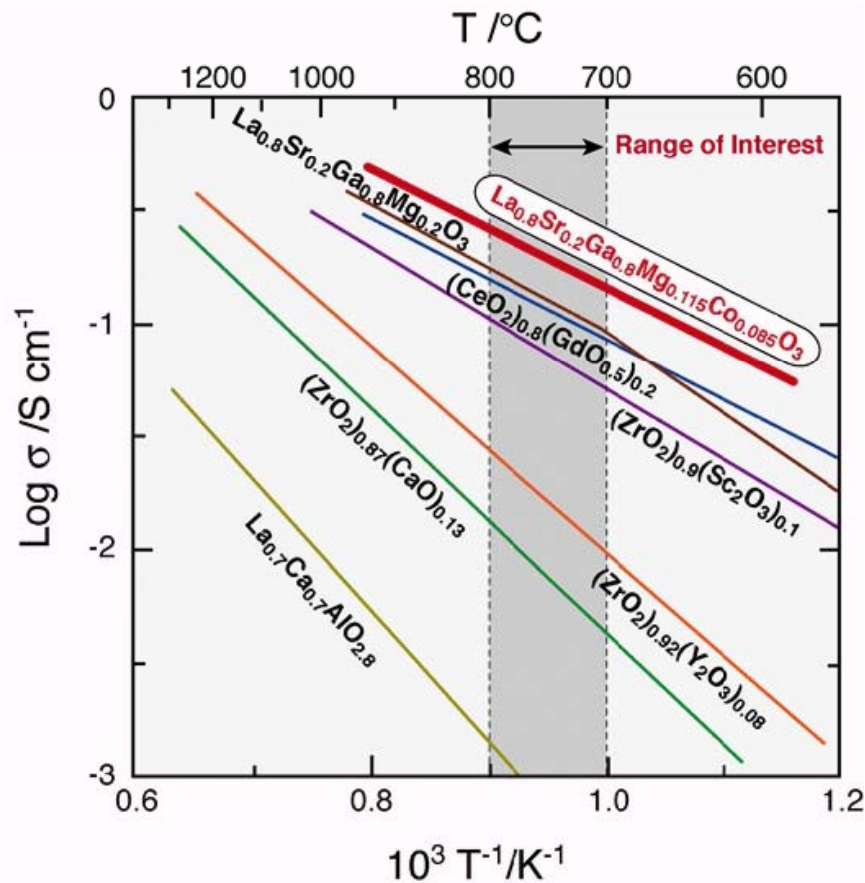
Change of barrier height

$$M = C \exp \left\{ -\frac{2}{\hbar} \sqrt{2m} \int_{x_0}^{x_1} \sqrt{\phi(x)} dx \right\}$$



Why can we move oxygen ions at room temperature ?

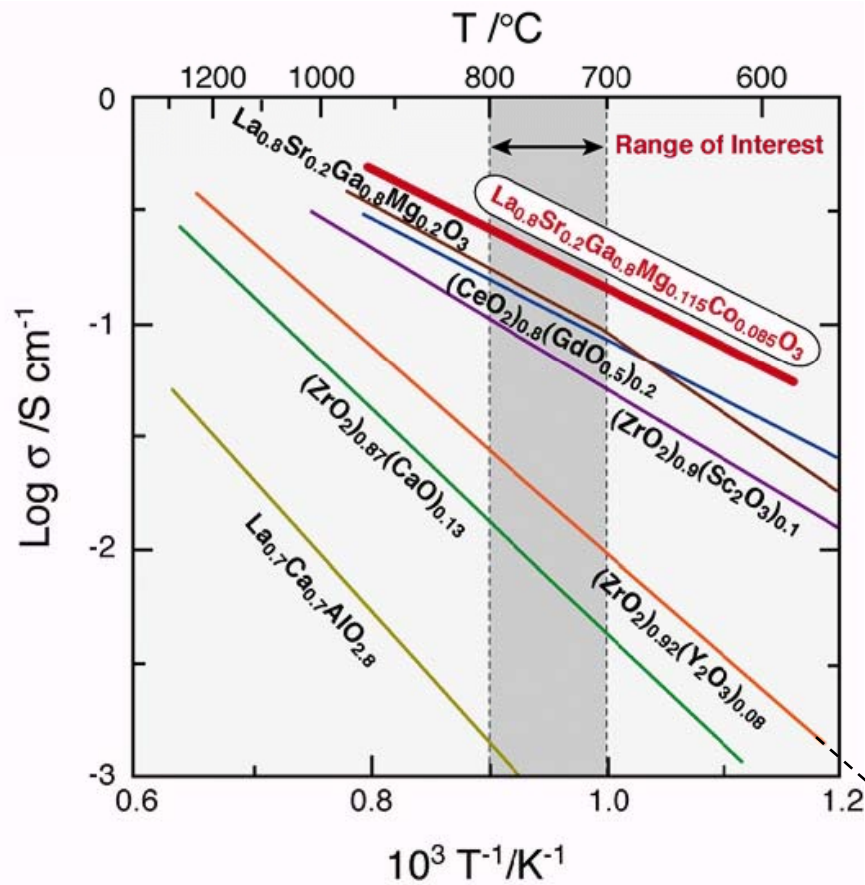
High temperature ion conductivity in oxides



From SOFC's we know that oxygen ions are only mobile at high temperatures.



Ion conductivity in oxides



Diffusion coefficient

$$D(T) = D_0 \cdot \exp\left(-\frac{H_A}{k_B T}\right)$$

(low field appr.)

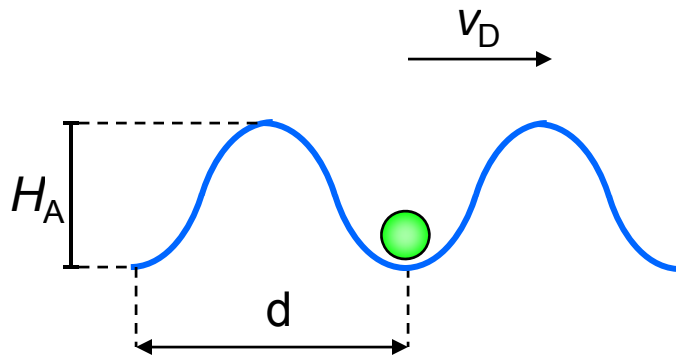
Oxygen mobility at room temperature is **too low**.

room temperature



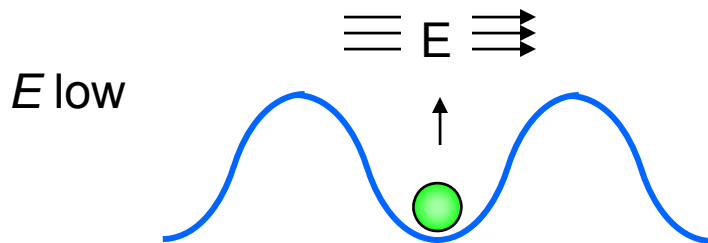
UNITY SEMICONDUCTOR

Drift velocity derived from atomic model



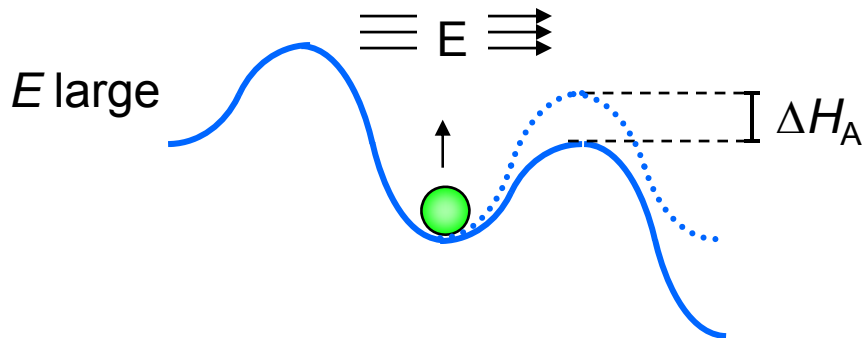
$$v_D = d\nu \exp\left(-E_a/kT\right) \left[\exp\left(\frac{qdE}{2kT}\right) - \exp\left(\frac{-qdE}{2kT}\right) \right]$$

drift velocity is *linear* with E-field



$$v_D \approx \frac{\nu d^2 qE}{kT} \exp\left(-E_a/kT\right)$$

drift velocity is *exponential* with E-field



$$v_D \approx d\nu \exp\left(-E_a/kT\right) \exp\left(\frac{qdE}{2kT}\right)$$



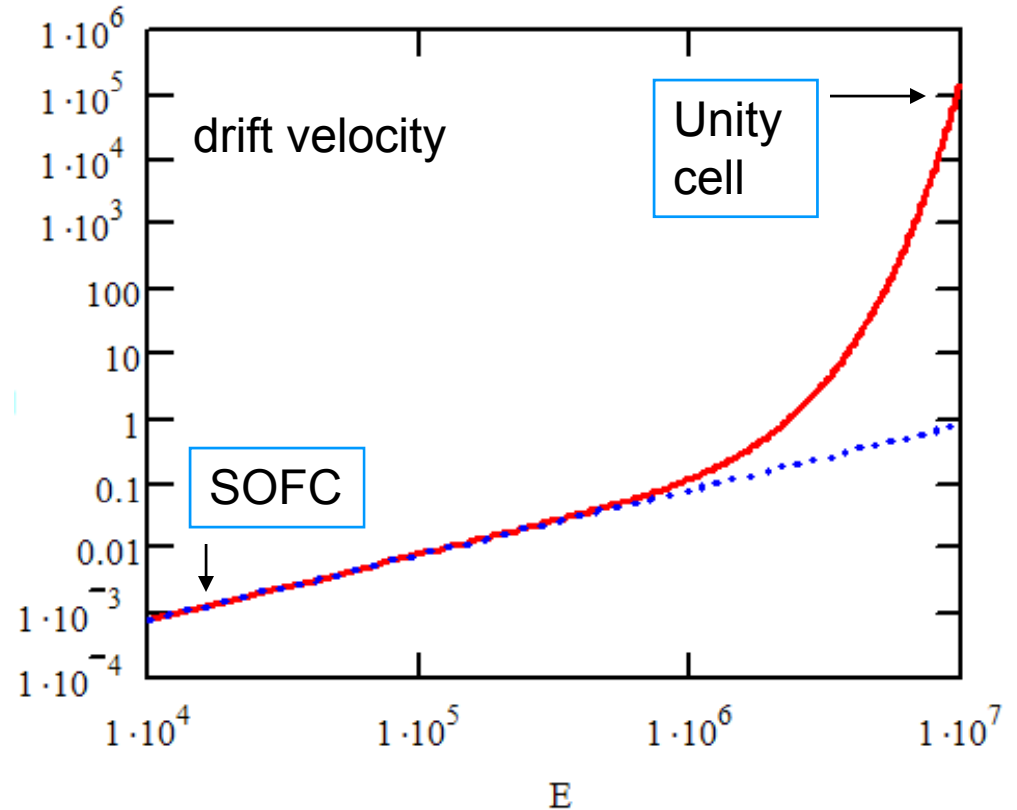
Ion drift velocity – linear vs. exponential solution

For high E-fields ($q_0dE \gg kT$):

$$v_D \approx d\nu \exp\left(-\frac{E_a}{kT}\right) \exp\left(\frac{qdE}{2kT}\right)$$

For low E-fields ($q_0dE \ll kT$):

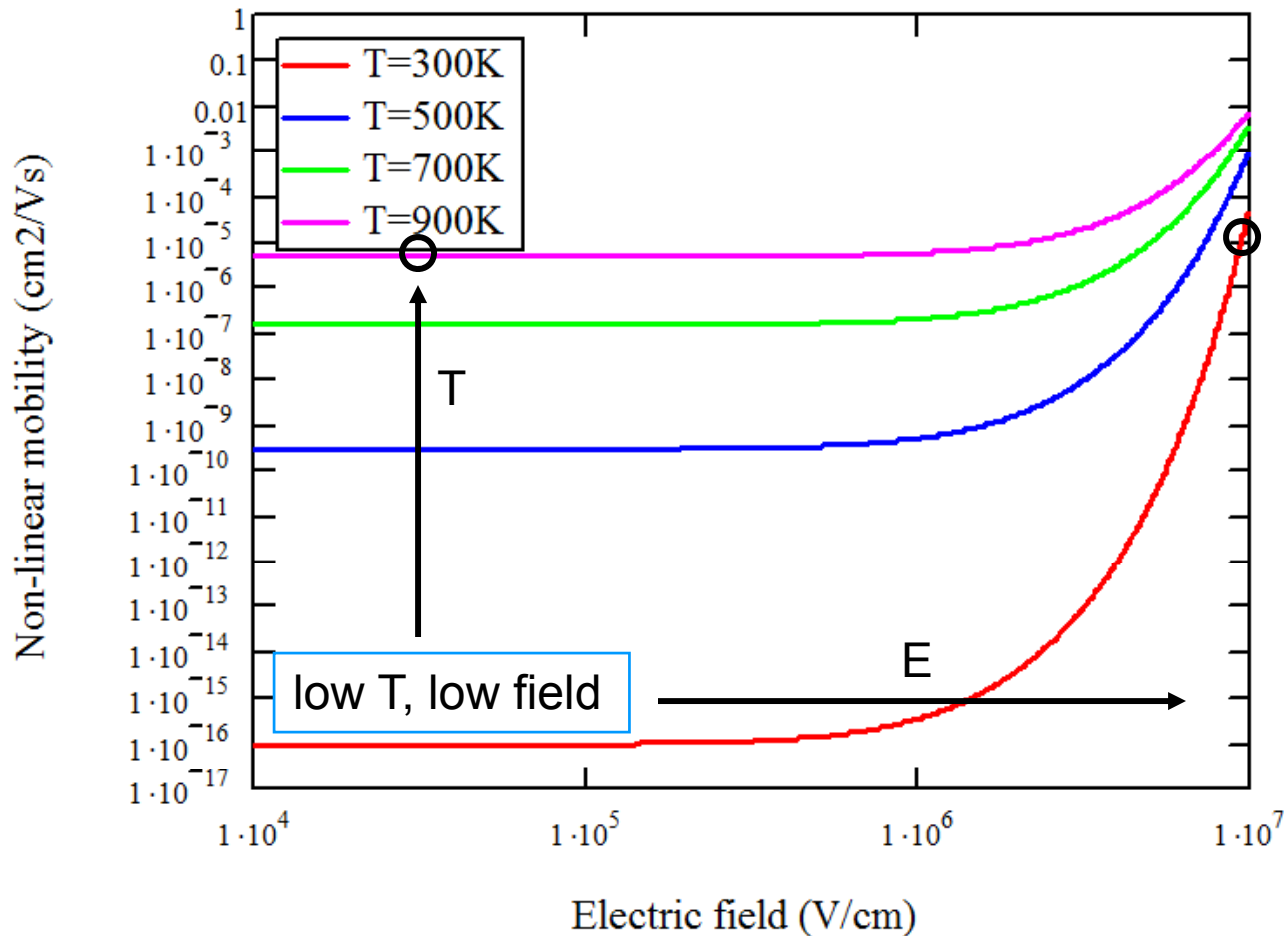
$$v_D \approx \frac{\nu d^2 qE}{kT} \exp\left(-\frac{E_a}{kT}\right)$$



Non-linearity effect kicks in at fields greater than 1MV/cm



Non-linear mobility at high electric fields

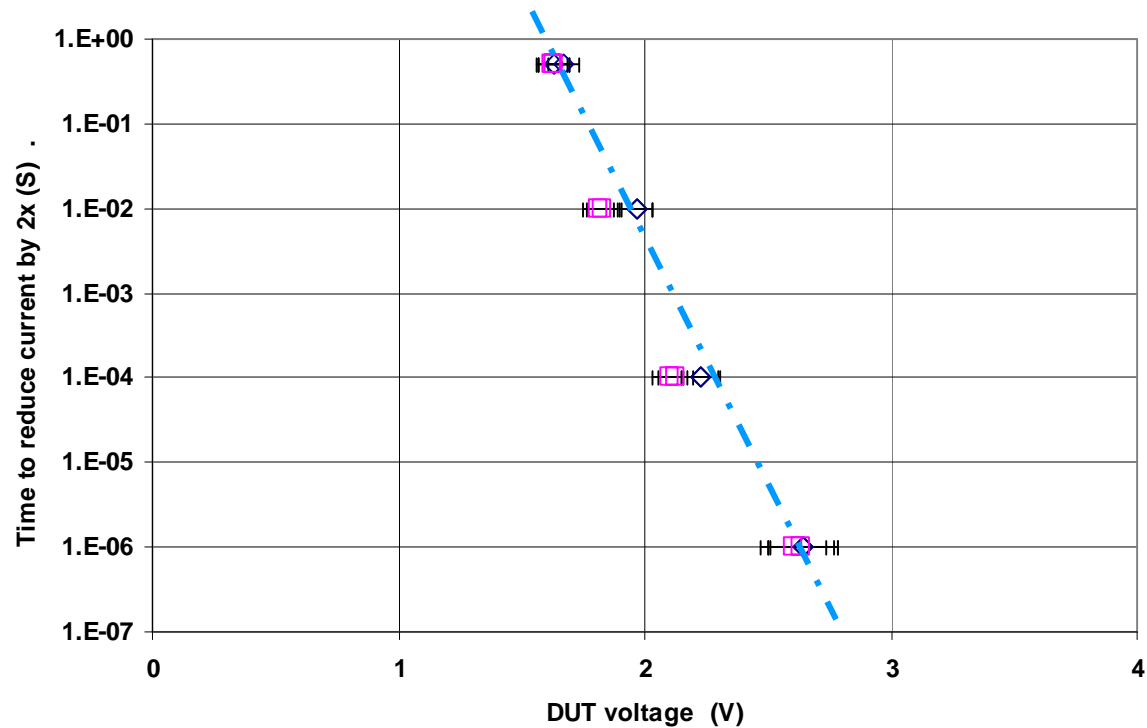


At high fields, however, ions mobility increases exponentially as a function of the electric field.



Electrical evidence for non-linear mobility

Programming time vs. programming voltage



Non-linear increase in ion mobility in our cell is considered a pure high-field effect. Heat is not involved.



Comparison: Unity vs. Binary Oxides

	Unity	Binary Oxides
- memory active area	uniform	filament
- electroforming	not required	needed
- device current is determined by	tunneling through deposited TB	under investigation
- p/e current scaling programming erasing	yes yes	no (?)
- current at a given area	TB thickness	(?)
- memory effect	redistribution of V_o	
- oxygen ion motion	E-field assisted	heat assisted (and E-field ?)
- resistance change due to	charge modulated TB height	under investigation
- memory operation	bipolar	unipolar/ bipolar



Unity Status

- Material choice and optimization is key:
 - A small subset of materials and material combinations was identified showing excellent cell performance.
- Deposition:
 - Low temperature budget required some processing tricks.
- Integration:
 - Maintaining oxygen stoichiometry is essential to prevent degradation of the cell performance.
 - etc.
- Conclusion:
 - There is still a lot work left to do.



Oxide Dual-Layer Memory Element for Scalable Non-Volatile Cross-Point Memory Technology

Rene Meyer, Lawrence Schloss, Julie Brewer, Roy Lambertson, Wayne Kinney, John Sanchez, and Darrell Rinerson
UNITY Semiconductor Corporation
Sunnyvale, CA-94085
rmeyer@unitysemi.com

Abstract— We report a dual oxide layer as the active memory element of a *scalable* nonvolatile cross-point memory technology. The resistance change memory element is formed by a conductive metal oxide adjacent to an oxide tunnel barrier. Varying the as-deposited tunnel barrier thickness allows for control of the nominal current density and is targeted to meet the cell requirements for an ultra high density cross-point architecture. Excellent scaling of program and erase currents with electrode area and a continuous transition between program and erase state indicate that a uniform rather than a filamentary switching mechanism controls the device current both in the high and the low resistive state. A prior forming step is not required.

The observed resistance change is caused by the exchange of oxygen ions between the conductive metal oxide and the tunnel oxide. Ion motion at room temperature is enabled by an exponential increase of the ion mobility under high electric fields during program and erase operations. The resistive switching effect of the device is explained by a change in the tunneling current due to an increase or decrease in effective tunnel barrier height. The barrier height varies due to changes in charge within the barrier as a result of oxygen ions moving in to or out of the tunnel barrier.

Keywords- *Nonvolatile Memory (NVM), Scalable, Cross-Point Technology*

I. INTRODUCTION

Recently, resistance change effects in metal oxides have gained increasing attention due to their potential to replace existing non-volatile memory technologies. Resistance switching has been reported in a large variety of materials ranging from binary oxides (e.g., TiO_2 [1] and NiO_2 [2]) to complex metal oxides like Cr-doped SrTiO_3 [3] and PCMO [4]. Different modes of operation such as unipolar and bipolar cycling as well as a wide range of operation voltages suggest that a variety of mechanisms might cause the resistance change. Most effects are related to the formation of a conductive filament. Local probe techniques (e.g., conductive AFM) have shown that the size of the filament defining the active area of the device is significantly smaller than the electrode area.

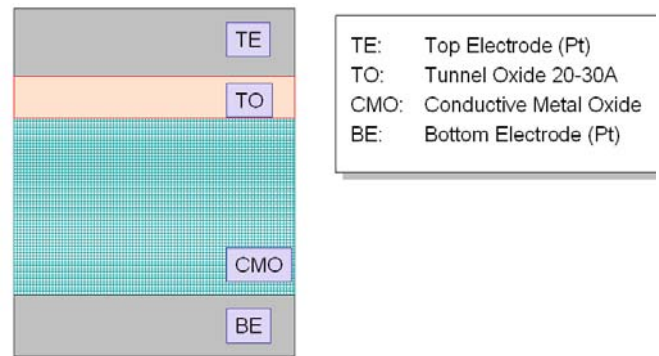


Figure 1. Schematic of the memory cell.

While the exact mechanisms are still being investigated, there is evidence that the resistance change effect in complex metal oxides is related to oxygen vacancy motion [3][5]. It is postulated that a redistribution of oxygen also plays a key role in other types of metal oxides. Little is known about how oxygen redistribution modulates the conductivity of the filament and how those devices can be scaled to smaller dimensions.

In this paper we discuss the basic structure and principle of operation of a scalable memory device used as the core element of Unity's CMO_x^{TM} cross-point technology. Tight specifications of 'on' and 'off' currents require adjustable cell current levels at a given technology node as well as current scaling of both the programmed and the erased state of the memory cell. A low temperature deposition process and a CMOS back-end-of-line integration scheme facilitate the building of two or more memory layers on top of each other to increase the memory density.

II. BASIC MEMORY STRUCTURE AND DEVICE OPERATION

A schematic of the basic cell structure is shown in Fig. 1. A metal bottom electrode deposited on a $\text{Si/SiO}_2/\text{TiO}_2$ wafer (or in some cases on a lattice matching single crystal substrate)

contacts a conductive metal oxide layer (CMO) of 250Å thickness. A tunnel oxide (TO) of 20Å to 30Å as shown in Fig. 1 is situated on top of the CMO. CMO and TO are deposited by rf-magnetron sputtering between 380°C and 450°C. Both films are fully crystalline with epitaxial (in case of a single crystal growth template) or columnar grain structure. Devices are formed by a patterned noble metal top electrode. Figure 2 shows a TEM cross section of the integrated device at different magnifications.

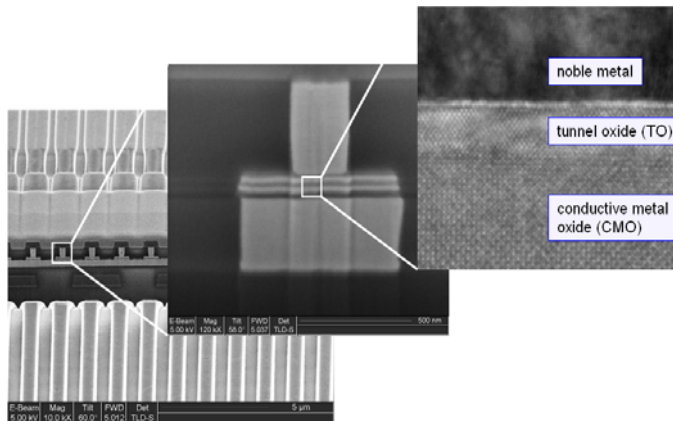


Figure 2. Cross section TEM of an integrated cell.

For all electrical measurements presented, the quoted voltage is applied to the top electrode; the bottom electrode is grounded. Positive and negative voltage sweeps were performed on untested devices.

Fig. 3 displays quasi-static I-V curves of memory devices as a function of the tunnel oxide thickness as well as the thickness dependence of the tunnel current at a given voltage. At voltages between -2V and 2V the I-V characteristic is essentially symmetric. Best fit of the I-V curve is found if we assume that the current-voltage relation follows a trap-assisted tunnel mechanism. Control of the tunnel oxide thickness allows tailoring of the device current levels according to technology and scaling requirements. Device characteristics are highly

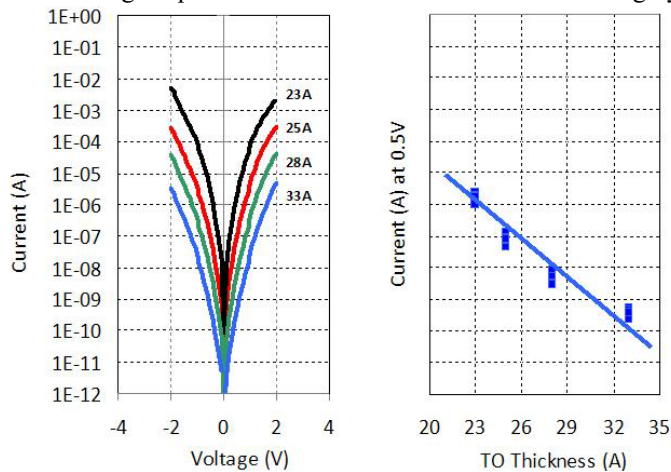


Figure 3. Memory cell characteristic as a function of tunnel oxide thickness and scaling of the current with tunnel oxide thickness.

reproducible and uniform across the wafer.

Voltages larger than 2V result in an asymmetric device characteristic, as shown in Fig. 4. For positive voltages the device resistance increases with increasing voltage causing the I-V characteristic to flatten. The high resistive state is further referred to as “programmed” state. Under higher bias, a negative differential current regime is observed. A decrease in current with increasing positive voltage is indicative of an increase in the device resistance. In this test the voltage is increased to breakdown for each voltage polarity. Positive and negative voltage sweeps were therefore performed on different devices. A closed loop voltage cycle shown in the inset Fig. 4 demonstrates I-V hysteresis, illustrating that the resistance change effect is fully reversible. It can also be seen that the resistance change after a positive voltage sweep is one to two orders of magnitude. Applying negative voltages causes an “erase” of the resistance change. During voltage stress, the resistance changes gradually, allowing intermediate resistance states. A distinct switching event and an abrupt change of the current, as found in many filamentary resistance change effects, is not observed.

After program and erase operations, the device retains the respective resistance state allowing it to function as a non-volatile memory element. The memory operation is bipolar, meaning that positive and negative voltages are required to switch between ‘on’ and ‘off’ states. In contrast to many binary oxides, an electroforming step is not needed.

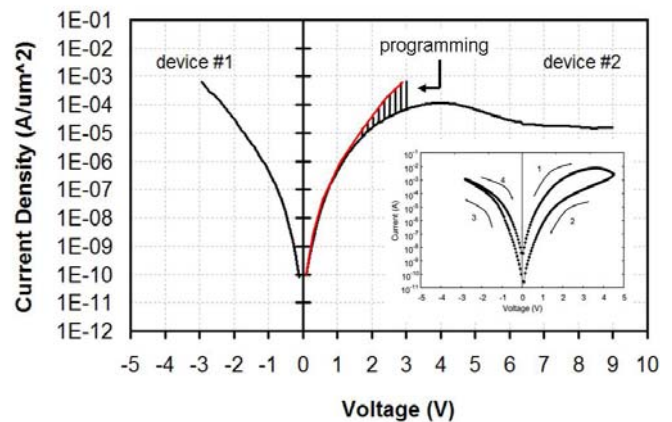


Figure 4. High field DC programming and I-V hysteresis of a memory device.

Applying bipolar voltage pulses causes a change in the resistance of ~10X. Program and erase cycle times have been found to depend exponentially on the pulse voltage. Typical operation voltages are ± 3V; typical pulse durations are 1µs to 10µs. Fig. 5 demonstrates open-loop cycling of a device. An interesting feature of the device is that the resistance change correlates with a capacitance change. Lower voltages result in significantly longer program/erase times or, for a constant pulse duration, in a reduced memory effect. Cycling endurance is ~10⁶ cycles. The current scaling with area is displayed in Fig. 6: initial, program and erase current all scale with area.

While a large variety of TO-CMO structures show a dc resistance change as reported in Fig. 4, only certain material combinations allow reliable device cycling in 10 μ s or less. Most materials degrade under the large electric fields required for device operation after only a few cycles.

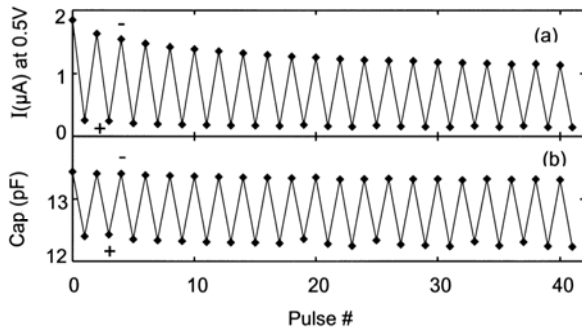


Figure 5. Open loop current cycling (a) and capacitance cycling (b).

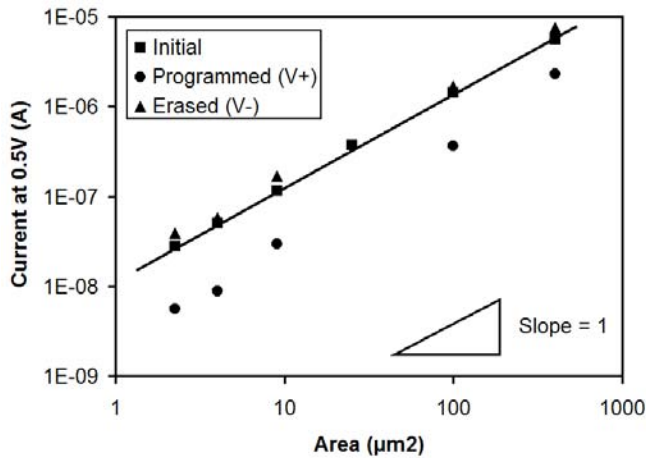


Figure 6. Area scaling of initial, program and erase state.

III. BASIC MEMORY MECHANISM

A. Ion transport in oxides

To understand the underlying mechanism of the resistance change, it is essential to consider both electronic *and* ionic transport processes in the tunnel oxide and the conductive metal oxide. Ion motion in binary and complex metal oxides at elevated temperatures is a well studied phenomenon [8]. Common applications are solid oxide fuel cells (SOFC) and oxygen sensors (Lambda sensors) used in automotive applications. In both cases, a solid state electrolyte (typically yttria-stabilized zirconia) conducts oxygen ions between electrodes. On a microscopic scale, ions are conducted through ion jump processes into oxygen vacancies or, less commonly, into oxygen interstitials. The particular mechanism depends on which disorder type (Frenkel-type or Schottky-type) is energetically more favorable in the crystal. Oxygen ion

transport processes are thermally activated with a motion enthalpy of 0.5eV to 1.5eV. At temperatures of 700°C and above, oxygen mobility is sufficiently high to enable ionic conductivity. In this temperature range the ion diffusion coefficient and basically the ion mobility follow an Arrhenius law:

$$D(T) = D_0 \exp\left(-\frac{E_A}{k_B T}\right), \quad (1)$$

where E_A denotes the migration enthalpy, D_0 is a temperature independent pre-factor and k_B and T are the Boltzmann coefficient and temperature, respectively. Ion (or vacancy) motion under electric fields is generally described by the particle mobility. The mobility can be calculated from the diffusion coefficient utilizing Nernst-Einstein's relation

$$\mu(T) = \frac{e_0 |z|}{k_B T} D(T). \quad (2)$$

Here z is the charge number of the ion and e_0 is the elementary charge. For an oxygen ion (O^{2-}) z equals to -2.

In case of a Schottky-type disorder it is beneficial to describe the diffusion of vacancies rather than of ions, since the ion diffusion coefficient depends on the number of vacant neighbors, while the diffusion coefficient of ion vacancies is independent of the defect concentration. For a detailed description refer to [8].

A reduction in temperature in Eq. 1 results in an exponential decrease of the ion mobility. At room temperature, oxygen ions are generally considered immobile. However, it has been shown that oxygen migration at room temperature can lead to a resistance degradation of ceramic capacitors if the capacitor is exposed to high unipolar voltages for extended periods [6]. A noticeable change in the performance of the capacitor as a consequence of oxygen ion drift may take several years at operating temperatures. Therefore, oxygen ions are not immobile at ambient temperatures but motion is typically considered to be very slow.

If the redistribution of oxygen causes the resistance to change in oxide memories, one must explain how oxygen can be moved within microseconds at room temperature. The answer is threefold: The first possibility is that, in case of a filamentary conduction mechanism, the high reset current combined with the very small area of the filament dissipates a significant amount of energy leading to local heating. In this case it seems likely that ion migration in filamentary memories is enabled by a heat assisted increase in the mobility. In case of the memory proposed in this paper, however, we have demonstrated that both program and erase current scale with area. An estimation of the temperature increase based on a heat transport model indicates that self-heating is *not involved*. Second, in our device, the distance oxygen ions are expected to travel is on the order of a few nanometers as opposed to many micrometers to millimeters for capacitor or fuel cells. However, this distance is still too far, if the ion drift increases linearly with the electric field.

This leads to a third possible explanation of the observed resistance change that requires a closer look at ion migration on

the atomic scale. Ion transport, on an atomic level, is described in terms of jump attempts (ν =attempt frequency, d =jump distance) over a potential barrier E_A . The drift velocity v_D of an ion under an electric field E is given by

$$v_D = \nu d \exp\left(-\frac{E_A}{k_B T}\right) \left[\exp\left(\frac{|z|e_0 d E}{2k_B T}\right) - \exp\left(-\frac{|z|e_0 d E}{2k_B T}\right) \right], \quad (3)$$

The relation between mobility and drift velocity defined by

$$v_D = \mu E \quad (4)$$

allows us to compare Eq. 3 with previous results derived from Eq. 1. For small electric fields, Eq. 3 can be approximated by

$$v_D \approx \frac{|z|e_0 \nu d^2 E}{k_B T} \exp\left(-\frac{E_A}{k_B T}\right) \quad (5)$$

The low field approximation reveals the drift velocity's linear dependence on the electric field, a results that is similar to Eq. 1. Under large electric fields, however, Eq. 3 simplifies to

$$v_D \approx \nu d \exp\left(-\frac{E_A}{k_B T}\right) \exp\left(\frac{|z|e_0 d E}{2k_B T}\right), \quad (6)$$

disclosing an exponential relation between drift velocity and applied electric field.

At room temperature and under small electric field load (Eq. 5), the kinetic (thermal) energy of an ion is too low to make a successful jump. Under large electric fields as described by Eq. 6, however, the potential barrier is lowered significantly, resulting in an exponential increase of successful jump events: ion mobility and, therefore, drift velocity increase exponentially under high electric fields. The effect of barrier lowering is similar to the field emission of electrons from a metal surface under high electric fields. In this case, the work function of the metal is lowered by the electric field.

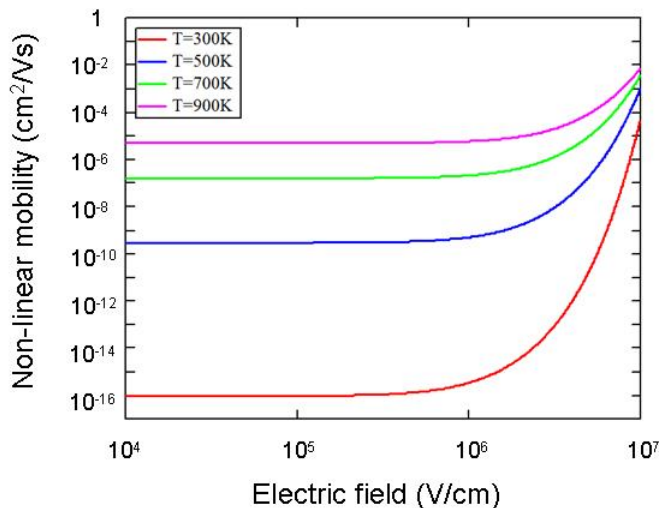


Figure 7. Ion mobility for a motion enthalpy of 1eV as a function of temperature and applied electric field.

Fig. 7 displays the mobility of oxygen interstitials (O^{2-}) in a metal oxide lattice calculated from Eqs. 3 and 4 for different

temperatures as a function of an external electric field. A motion enthalpy of 1.0eV was assumed. For electric fields smaller than 100kV/cm, the mobility is only a function of temperature. Compared to 900K the room temperature mobility drops by 10 orders of magnitude. The non-linearity of the mobility sets in at around 1MV/cm such that under electric stress fields close to 10MV/cm the mobility at room temperature approaches values of the low field mobility at 900K. Based on the atomic model for ion motion in solids, oxygen ions can move at room temperature if sufficiently large electric fields are applied. At 10MV/cm, mobility at room temperature is about 10^{12} orders of magnitude greater than the low field mobility. However, only certain metal oxides can withstand such electric fields without degradation.

B. Oxygen exchange between TO and CMO

With regard to ion motion, the tunnel oxide used in our structure acts as a solid state electrolyte and the conductive metal oxide acts as a mixed ionic electronic conductor. At program and erase voltages of 2-3V and a tunnel oxide thickness of 20-30Å, an electric field on the order of 10MV/cm is generated in the tunnel barrier. Over the distance of the screening or Debye-length of a few nm, the electric field also penetrates the conductive metal oxide. Due to the high field present in the TO and CMO, oxygen ions can be exchanged between tunnel oxide and conductive metal oxide over small distances even at room temperature. Fig. 8 illustrates the oxygen ion exchange between CMO and TO for positive voltages applied to the top electrode.

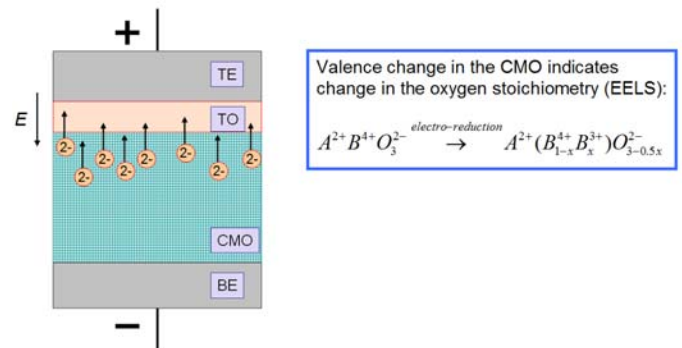


Figure 8. Illustration of the “programming” operation of the memory device. Under sufficiently high electric fields O^{2-} ions are redistributed from the CMO into the TO.

Under positive fields oxygen O^{2-} is moved from the CMO into the TO. Negative fields cause migration of oxygen from the TO back into the CMO.

Indirect evidence for oxygen ion motion was found by studying the cation valence change in the CMO by EELS techniques before and after programming. After programming of the device the B-site cation valence changed to a lower valence state indicating a loss of oxygen in the CMO.

C. Resistance change effect

Resistance changes in the memory device can now be understood in terms of variations in the density of trapped

charge in the tunnel oxide. In our case the trapped charge is oxygen ions. During “programming” (positive voltage applied to the top electrode) an increase in the device resistance is observed. Oxygen ions migrate under high fields from the CMO into the TO and excess negative charge accumulates in the TO. As a consequence, electrons tunneling through the TO are repelled by the negative charge in the tunnel barrier: the tunnel current decreases as the tunnel barrier height increases. An “erase” pulse (negative voltage to the top electrode) forces oxygen ions to move out of the TO into the CMO. The reduction of negative charge in the TO leads to a lowering of the effective tunnel barrier and an increase in the tunnel current. An illustration of the shape of the tunnel barrier potential for the “programmed” and “erased” state is shown in Fig. 9. In conclusion, the resistance change effect is caused by a space charge modulated tunnel current. The modulation of the space charge in the tunnel barrier is due to an accumulation (“program”) or depletion (“erase”) of negatively charged oxygen ions in the tunnel oxide. Oxygen migration at room temperature is enabled by a non-linear increase of the mobility under high electric fields.

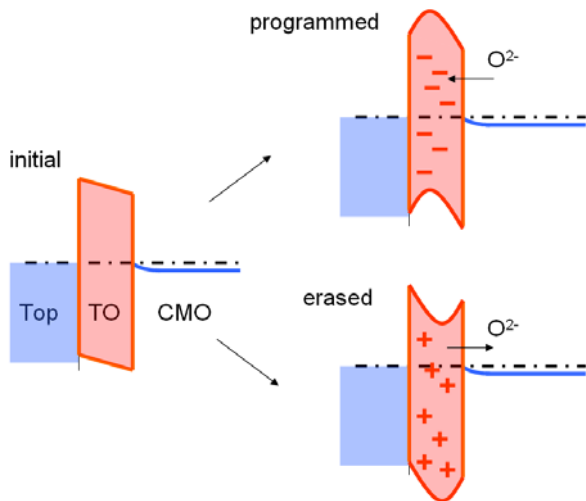


Figure 9. Sketch of the potential barrier for initial, programmed and erased memory cell.

Numerical methods are employed to understand oxygen ion motion across the TO-CMO interface in more detail. A transient solution of the transport problem is obtained by solving the non-linear transport equations and continuity equation for oxygen vacancies, oxygen interstitials, and electronic charge carriers. This is performed in combination with Poisson’s equation and appropriate boundary conditions describing the electrodes and the TO-CMO interface. The method applied here is similar to that described in Ref. [7]. As an example, the evolution of the oxygen vacancy profile with time during “programming” is illustrated in Fig. 10.

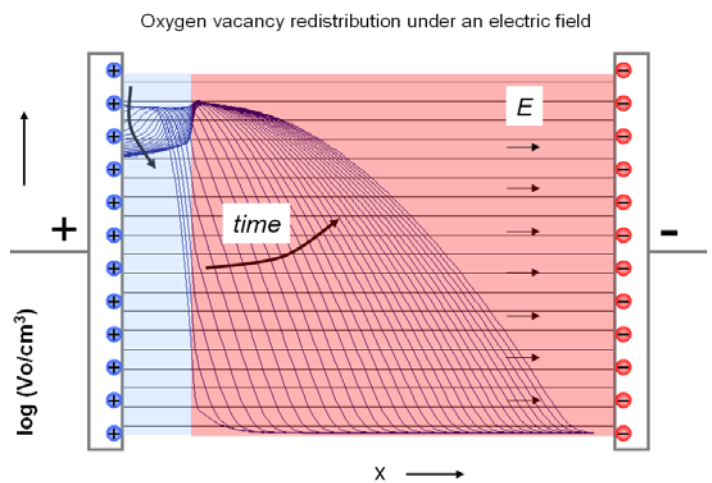


Figure 10. Simulated evolution of oxygen vacancy profile with time during “programming”.

IV. SUMMARY

A new memory structure for resistive information storage is proposed, in which the memory is formed from a conductive metal oxide CMO and an intentionally deposited tunnel oxide TO. We have found that in this structure program, erase and read current scale with area. Current scaling, key for the integration in a *scalable* cross-point technology, differentiates this device from other switching binary and complex oxides, where memory functionality relies on a formed conductive filament. In addition, current levels for devices with identical electrode area depend exponentially on the thickness of the tunnel oxide. This feature allows us to adjust the cell current to meet the memory cell requirement of a cross-point architecture. An electro-forming process, which is required for filamentary-type memories to form a conductive filament, is not needed.

The memory effect is explained by an exchange of oxygen between the CMO and the TO. In contrast to resistance switching in binary oxides, an exponential increase in the mobility is caused by high electric fields rather than self-heating of the memory cell. The memory cell resistance changes as a function of the concentration of oxygen ions in the tunnel barrier. The ionic space charge in the barrier affects the tunnel current by modulating the tunnel barrier height.

REFERENCES

- [1] D. B. Strukov, G. S. Snider, D. R. Stewart, R. S. Williams, *Nature* **453**, 80-83 (2008).
- [2] J.-B. Yun, S. Kim, S. Seo, M.-J. Lee, D.-C. Kim, S.-E. Ahn, Y. Park, J. Kim, H. Shin, *Phys. Stat. Sol.* **1**, 280-282 (2007).
- [3] M. Janousch, G. I. Meijer, U. Staub, B. Delley, S. F. Karg, B. P. Andreasson, *Adv. Mater.* **19**, 2232-2235 (2007).
- [4] S.Q. Liu, N.J. Wu, and A. Ignatiev, *Appl. Phys. Lett.* **76**, 2749 (2000).
- [5] K. Szot, W. Speier, G. Bihlmayer, R. Waser, *Nature Mater.* **5**, 312 (2006).
- [6] R. Waser, T. Baiatu, K.-H. Haerdtl, *J. Am. Ceram. Soc.* **73**, 1645 (1990).
- [7] R. Meyer, R. Liedtke, and R. Waser, *Appl. Phys. Lett.* **86**, 112904 (2005).
- [8] J. Maier, *Physical Chemistry of Ionic Materials: Ions and Electrons in Solids*, John Wiley & Sons Inc (2004).